

# Phase Locked System Design and Measurement Tutorial Consisting of Physical Hardware and Co-simulation Environment.

Martin John Burbidge<sup>1,2</sup>

<sup>1</sup> Faculty of Applied Sciences, Lancaster University, Lancs UK, LA1 4YR

<sup>2</sup> Institute of System Level Integration, Alba Centre, Alba Campus, Livingston, Scotland, UK

email: m.burbidge@lancaster.ac.uk

## *Abstract*

Phase locked loop based feedback techniques are used in a variety of system level timing, control and communication applications. Re-configurable hardware and associated simulation models have been developed with an emphasis towards teaching the fundamentals of Phase locked loop systems. The material is hardware focussed and reinforces, control system theory, characterisation, design, and modelling. The simulation part of the material can be used in an Internet based teaching environment. Keywords: Phase locking, Phase locked loops, Behavioural system modelling, Control systems, Hardware verification.

## **1. Introduction**

Phase locked loops (PLL) and associated phase locking theory are important and useful techniques that can be used in a variety of electronic communications, control and instrumentation applications. Techniques are widely used in larger systems that require precise timing or control reference signals that are directly synchronised to a system output. Typical applications include motor speed control<sup>1, 2</sup> and RF (Radio Frequency) carrier generation<sup>3</sup>. Various types of phase locked architectures exist encompassing fully Analogue, Semi digital, and fully digital types<sup>2</sup> of PLL respectively. It must be noted that although the term digital is used the transient response of the PLL control parameters during acquisition is essentially an analogue phenomenon. In terms of popularity the semi digital type of PLL or charge pump phase locked loop (CP-PLL) seems to be the architecture of choice for the majority of current hardware based phase locking applications. This type of PLL is readily and cheaply available as a stand-alone building block, and can be configured to have similar transient response to other types of PLL.

The PLL is essentially a closed loop feedback control system and can, depending on the implementation, be compared and contrasted with classic feedback control systems, such as proportional plus integral (PI) feedback loops. Many key PLL references rely heavily on classic control system theory and they often provide mechanical analogies to help explain PLL operation. All common control system design techniques, for instance, bode plots, step response plots, nyquist plots, and s domain mapping<sup>4</sup>, can be used to aid the engineer in realising a correct system PLL implementation. However, a PLL system differs in one significant aspect, which is that the inputs and

outputs of the system are usually considered to be continuous periodic signals as appose to a constant parameter. The PLL system essentially measures the phase difference (and sometimes frequency difference) between the two continuous signals and activates the feedback mechanism accordingly until the respective signals are phase aligned. This change from operating on an ideally constant parameter in the steady state (voltage, force, displacement, current, etc) to that of a constant parameter relating two continuously time varying signals (i.e. phase) can lead to confusion when attempting to explain phase locking theory and applications. In consequence it can deter students from fully appreciating the processes involved.

Despite their widespread use in industrial applications, PLL system techniques seem to be only superficially covered in many general undergraduate electronic / mechatronic course. Structured practical examples and experimentation can be used to enhance theoretical understanding of this useful technique and also provide a good reinforcement of essential elements of classic control theory. Furthermore, linking of basic theory to experiments can provide potential practising engineers with a sound working knowledge of the system.

With the previous points in mind the attempt was made to see if any available material applicable to teaching applications was freely and cheaply available. Various simulation / modelling packages are available on the market and some of these include PLL models. However, it was a major objective of the envisaged course to include a significant proportion of practical experiments and measurements on physical hardware. Many of the available simulation models are generic in nature and are not wholly applicable to the specific task. Another problem was that of selecting a suitable hardware demonstrator. Many PLL manufacturers supply demonstration boards for their PLLs and also have excellent accompanying design tools<sup>5, 6</sup>. Unfortunately, due to many reasons, such as expense and complexity, many of the boards were unsuited for general teaching applications.

The decision was made to develop a complete set of course notes, simulation models and hardware to allow students to carry out a set of measurements and experiments relating to PLL measurement and design. In the initial stages of course development a set of primary requirements and student objectives were decided upon. These are highlighted below.

- The course must be self-contained and include sufficient theoretical material to provide an initial working knowledge of phase locking theory.
- The course must provide the student with a practical working knowledge of PLL systems.
- The course must ease the student's assimilation of further advanced feedback system theory.
- The course must reinforce current control system knowledge through example and experimentation.
- Material must contain a significant hardware element. Thus allowing students to carry out real measurements and experiments on electronic systems that are applicable to real world applications.
- Material must contain a complementary set of simulation models that relate to the physical hardware system.
- The course must emphasise that simulations are not reality, and thus encourage the student to investigate the differences between the two domains.
- Material should identify basic functional hardware system checks that should always be carried out during system debugging.
- The course must provide an indication of behavioural modelling and simulation techniques related to phase locking and control systems.
- The course must provide students with examples of oscilloscope measurement techniques and oscilloscope to personal computer data connectivity options.

From the above requirements the material was split into two distinctive parts, consisting of a set of simulation models and background theory and a hardware evaluation platform, respectively. The developed hardware includes a set of accompanying notes that explains equipment set-ups, and measurement procedures. In addition technician's notes and required components for each experiment are documented. Also, an appendix section is included that contains further set-up details and a cross-referenced schematic of the hardware demonstrator.

The resulting developed course material is designed to be used in the following manner. Initially, the student is expected to carry out the simulation aspect of the course remotely prior to attending the lab-based sessions. The simulation part of the course is designed to be used in a web / Internet based teaching environment. During this phase the student is encouraged to modify various aspects of the simulation models and observe the results. Also, the student is expected to become familiar with the lab notes and appendices. Both the simulation and lab-based exercises allowed the student to carry out general system level characterisation experiments such as, transient step response monitoring and, closed loop transfer function monitoring. These types of experiments are also representative of those that would be used for design and evaluation of generic control systems. In addition, PLL specific tests are carried out, such as, VCO (voltage controlled oscillator) gain and linearity, and open loop VCO noise related measurements.

All of the above measurements can be carried out in both the simulated and real environment. However, results may differ slightly between the domains due to natural component deviations. The students are encouraged to investigate the perceived differences between measured and simulated results. Further measurements essential to hardware evaluation concentrate on typical system level tests. These include power supply (component supply voltage measurements, and basic signal frequency and voltage measurements. These aspects are not included in the simulation environment. A recommendation for ordering of the course material is given and is outlined as follows.

1) Simulation exercises and familiarisation with lab notes. 2) Basic hardware testing. 3) VCO gain testing. 3) Transfer function monitoring. 4) Step response monitoring.

A strict requirement of the ordering is that the basic hardware testing (item 2) must be carried out before other hardware characterisation.

Response monitoring and measurement is carried out via use of an Agilent 54622D<sup>7</sup> oscilloscope connected to a personal computer. Signal generation is carried out using an Agilent 33120A<sup>8</sup> arbitrary waveform generator. Specific spreadsheets with incorporated equations have been developed to allow automatic plotting of the PLLs transfer function and VCO gain. Assessment is primarily carried out via comparison of the student's results for particular experiments against pre-calculated results. In addition, suitable questions are included to assess the students understanding of key concepts.

Subsequent sections of this paper are used to provide more detailed examples of the course material. An overview of the section content is provided below.

Section 2, is used to introduce the PLL simulation models. The section also provides an overview of basic PLL theory required for the course. In addition, analytical and simulation plots relating to PLL operation are shown.

Section 3, provides an outline of the hardware board and describes the associated functionality. This is followed by a summary of typical background theoretical material that is included in the lab session. A schematic representation of a typical test set-up is then shown. The section also outlines the test procedure and lab documentation for a transfer function test. Typical Excel™ results and example questions are also documented.

Finally, section 4, is used to summarise the paper.

## 2. Simulation models and PLL descriptions and example output response.

The primary purpose of the simulation-based parts of the course are to provide the student with behavioural and analytical models that correspond to material included in the practical sessions. Phase locked loop simulation models are investigated with reference to the practical course material. This is done so that the student can gain some familiarity with the test methods prior to attending the practical sessions. The material in this module is also used to summarise the key equations relating to the course.

An overview of the contents of the simulation based module is provided as follows;

1) Spice PLL model, operational explanation and general equations; 2) Standard analytical models for frequency step response and transfer function response; 3) Simulations of various PLL blocks including; (a) Phase detector and loop filter; (b) VCO (Voltage controlled oscillator); 4) Spice simulation for step response; 4) Spice simulation for phase transfer response.

Mixed mode (SPICE and XSPICE) models for the PLL models used in the course were developed within the B2SPICE<sup>9</sup> simulation package. Further models were developed for use in the SMASH<sup>10</sup> EESOF<sup>11</sup> and SPECTRE<sup>12</sup> simulation environments. It is the intention that the additional models are used in a more advanced course related to RF modelling and design. The analytical models were developed for use in MATLAB<sup>13</sup> and OCTAVE<sup>14</sup>.

### 2.1. Simulation model explanation and key equations.

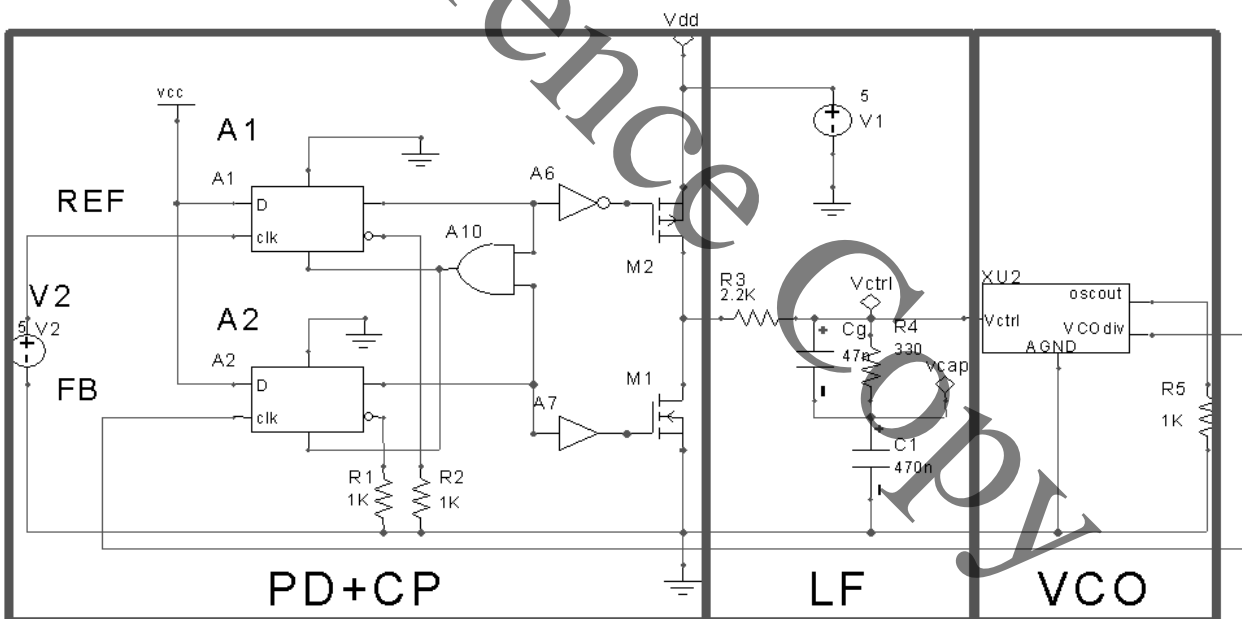


Figure 1 Illustration of the PLL simulation model.

The circuitry depicted in figure 1 represents a mixed signal model of the 74HCT4046<sup>15</sup> Charge Pump Phase locked loop that is used for the practical exercises. The key elements of the simulation model are explained below along with their respective parameters. The information in this section is only intended to provide a brief overview of the key PLL sub sections, further more detailed information on PLL operation is provided in<sup>2,3</sup>.

1) **PD+CP:** This part of the circuit models the **Phase detector** and **Charge-Pump** respectively.

**a. Phase Detector:** The purpose of the phase detector is to produce correction signals at its outputs (see M2 and M1) that are proportional to the difference at its inputs (see A1 clk and A2 clk). Note that the phase detector in this circuit only operates on rising edges of the input signals. Also this type of phase detector has a detection range of  $\pm 2\pi$  ( $360^\circ$ ). This statement can be proved by experimentation with the provided simulation models.

**b. CP:** The charge pump circuit converts the outputs from the phase detector into voltage signals that are directly proportional to the phase difference on the PLL inputs.

The voltage source V2 is used to generate the phase locked loop reference signal (REF). The associated gain of the phase detector and charge pump together is usually expressed as  $K_d$  where:

$$K_d = \frac{V_{cp\max} - V_{cp\min}}{4\pi}$$

**Equation 1 Phase detector and charge pump gain.**

Where:  $V_{cp\max}$  is the maximum voltage the charge pump output transistors can rise to before saturation and  $V_{cp\min}$  is the minimum voltage the charge pump output transistors can fall to before they switch off.

For the particular circuit we are interested in the output of the phase detector is approximated as 0.4 v/r (volts per radian)

This value is taken from the data sheet for the 74HCT4046AN PLL<sup>14</sup>. The student is recommended to refer to this data sheet.

**2) LF: Loop filter:** The basic function of the loop filter is to provide a filtering action on the PLL input signal and other higher frequency terms in the signal that are produced due to the phase detector action. Generally in the steady (or locked) state the loop filter output should be a stable voltage that is suitable for the control of the VCO.

With reference to the simulation model, the transfer function of the loop filter for this particular PLL is provided below.

$$F(s) = \frac{1 + \tau_2}{s(\tau_1 + \tau_2)}$$

**Equation 2 Loop filter transfer function.**

Where:

$$\tau_1 = R3 \cdot C1 \text{ (s)}$$

**Equation 3 Calculation of t1**

And,

$$\tau_2 = R4 \cdot C1 \text{ (s)}$$

**Equation 4 Calculation of t2**

Note: A small deglitching capacitor  $C_g$  is included in the loop filter network. For the purpose of analysis and analytical models used in later sections its action upon coarse overall PLL response can be omitted.

**3) VCO: Voltage Controlled Oscillator:** The purpose of the VCO is to produce a periodic output signal whose frequency is proportional to its input voltage.

The gain of the VCO is a measure of how much the output frequency of the VCO changes with respect to a change in input voltage i.e.

$$K_{vco} = \frac{\Delta\omega}{\Delta V} \text{ (rps/v) (radians per second per volt)}$$

**Equation 5 VCO gain equation**

Note: that  $K_{vco}$  is often given in units of r/s/v, however in certain circumstances it is better to give the value in terms of Hz / v. Equation 5 can be converted to Hz/v by dividing by  $2\pi$ .

**4) Loop divider:** This is not shown in the simulation model, however most practical CP-PLL synthesisers include some form of feedback divider network. The feedback network usually changes the VCO frequency to a lower frequency before it is fed back to phase detector input. Assuming that all the other parameters are set up correctly, inclusion of a feedback divider allows the PLL to generate and output a signal that is an integer multiple of the reference signal supplied to the PLL i.e.

$$F_{out} = N \cdot F_{in} \text{ (Hz)}$$

**Equation 6 Relationship between PLL output frequency and input frequency for integer divider ratio.**

Where:  $F_{out}$  is the frequency of the PLL output signal,  $F_{in}$  is the frequency of the PLL input signal or reference signal, and  $N$  is the value of the divider.

Equation 6 represents the key basic equation for the CP-PLL when it has reached steady state operation. Ideally when the PLL is operating correctly and when it has reached its steady state operation the output frequency will be  $N$  ( $N \neq 0$ ) times the reference frequency.

The actual PLL circuit used in the practical sessions contains a feedback divider constructed from a digital counter. This element is highlighted in the hardware description section of section 3. In the simulation model the division ratio is incorporated directly into the VCO description via use of a specific equation. This method produces realistic simulation results and also drastically reduces simulation times.

For transient response and transfer function calculations, the PLL system is often expressed in the Laplace domain in terms of natural frequency ( $\omega_n$ ) and damping ( $\zeta$ ). Where  $\omega_n$  and  $\zeta$  are derived from the particular system parameters. For completeness the normalised Laplace equations for a high gain second order PLL circuit is provided in equation 7.

Using feedback theory it can be shown that the closed loop transfer function for the PLL used in the exercises can be expressed as follows.

$$\frac{\theta_o(s)}{\theta_i(s)} = H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

**Equation 7 Transfer function for second order PLL.**

Where:  $\theta_i$  is the phase of the input signal.  $\theta_o$  is the phase of the output signal.  $\omega_n$  is the natural frequency of the system in radians per second and  $\zeta$  is the damping factor of the system.

Equation 7, can be compared to equations found in classic control theory texts<sup>1, 4</sup>. However, when carrying out any analysis it must be remembered that the inputs and outputs of the system are now in terms of phase.

For the circuit in question  $\omega_n$  and  $\zeta$  can be defined as follows:

$$\omega_n = \sqrt{\frac{K_O K_{PD}}{N(\tau_1 + \tau_2)}}$$

**Equation 8 Estimation of natural frequency from circuit parameters.**

and

$$\zeta = \frac{\omega_n \tau_2}{2}$$

**Equation 9 Estimation of damping factor from circuit parameters**

MATLAB files are included as part of the course material that allow calculation of equations 8 and 9 directly from the loop filter component values.

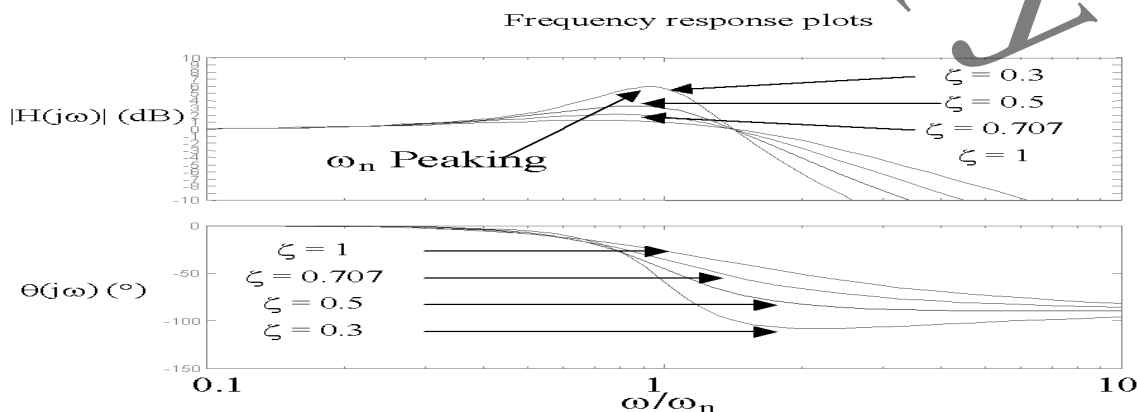
The natural frequency and damping of the loop will control the transient response of the loop (including settling time and overshoot) and will also have direct control over the loop bandwidth. More information about the natural frequency and damping is provided in the hardware based course modules.

The key equations required to carry out the course material adequately are 3, 4, 5, 6, 8, 9. Other equations are included for completeness and to provide more advanced students with an initial point of reference for Laplace based representations of control systems. The main reason for this approach is that it was desired for the material to be applicable to a wide range of students and prior knowledge of Laplace domain calculations could not be guaranteed. An important focus of the course is to show a qualitative relationship between component values, natural frequency and damping and to allow the student to observe output response changes.

## 2.2. Example analytical response curves.

In many situations the initial part of the design phase starts with a specification for desired final system performance. With a PLL, typical design issues centre on bandwidth, and transient response of the final system when it is subjected to certain inputs. Commonly used inputs that can allow frequency and transient response to be calculated are sinusoidal frequency modulation and frequency steps, respectively. It is common to find normalised frequency response plots and transient response plots of systems reproduced in PLL and control system texts.

A normalised transfer function plot included in the course material is shown in figure 2.



**Figure 2 Normalised PLL transfer function plot.**

The plot of figure 2 shows magnitude and phase response of the output signal of a second order PLL when it is subjected to an increasing input modulation frequency. That is, the continuous periodic input signal is phase or frequency modulated at increasing modulation frequencies. Plots are created in MATLAB and using equation 7. A copy of the code listing that will generate the normalised transfer function plots is included as part of the course material.

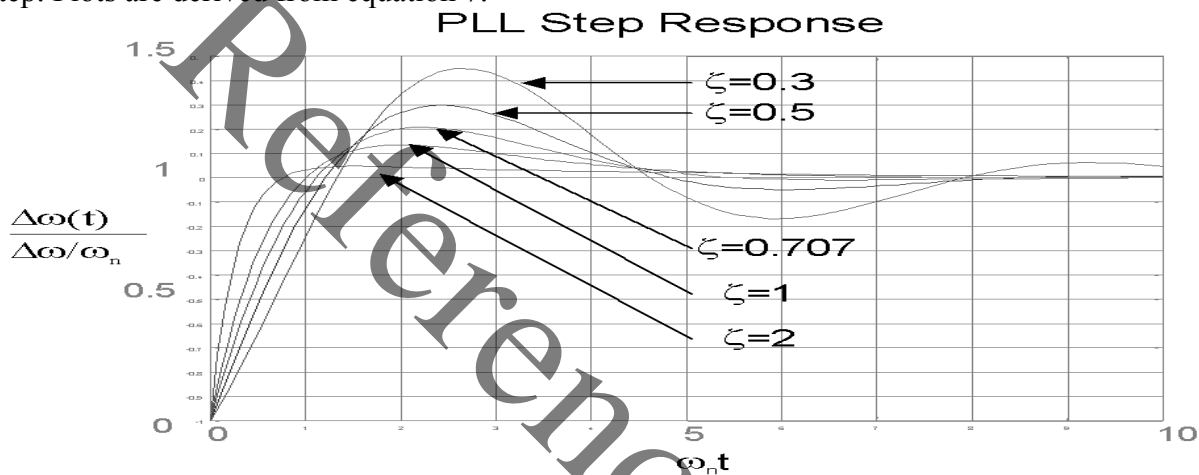
Note that the transfer function can also be plotted manually by making the substitution.

$$s = j\omega$$

**Equation 10** Substitution for manual transfer function plotting.

Into equation 7.

Figure 3 show normalised PLL step response plots when the PLL is subjected to an input frequency step. Plots are derived from equation 7.



**Figure 3** Normalised PLL step response plots for input frequency step.

Both of the plots shown in figures 2 and 3 may be used to aid estimation of component values.

For instance a final system may be specified to have the following characteristics.

Settling time  $\leq 1ms$  to 5% of the steady state value.

Overshoot  $< 30\%$  over the steady state value.

If we initially choose the plot for  $\zeta = 0.707$  from figure 3 the overshoot is approximately 20% (from the graph) this will give a suitable safety margin.

Then inspection of the graph shows that the selected curve has settled to within 5% for:

$$\omega_n t = 8$$

Therefore the required value for  $\omega_n$  is

$$\omega_n = 8/t = 8/1ms = 8kr/s$$

**Equation 11** Example calculation for natural frequency from step response graphs

Estimated values for the natural frequency and damping can be used in conjunction with equations 8 and 9 to aid selection of system component values.





In figure 5 the lower trace shows a scaled version of the FM (Frequency Modulated) control input to the PLL, the uppermost trace containing transient spikes is the loop filter control voltage, and the smooth uppermost trace is the voltage on the main loop filter capacitor.

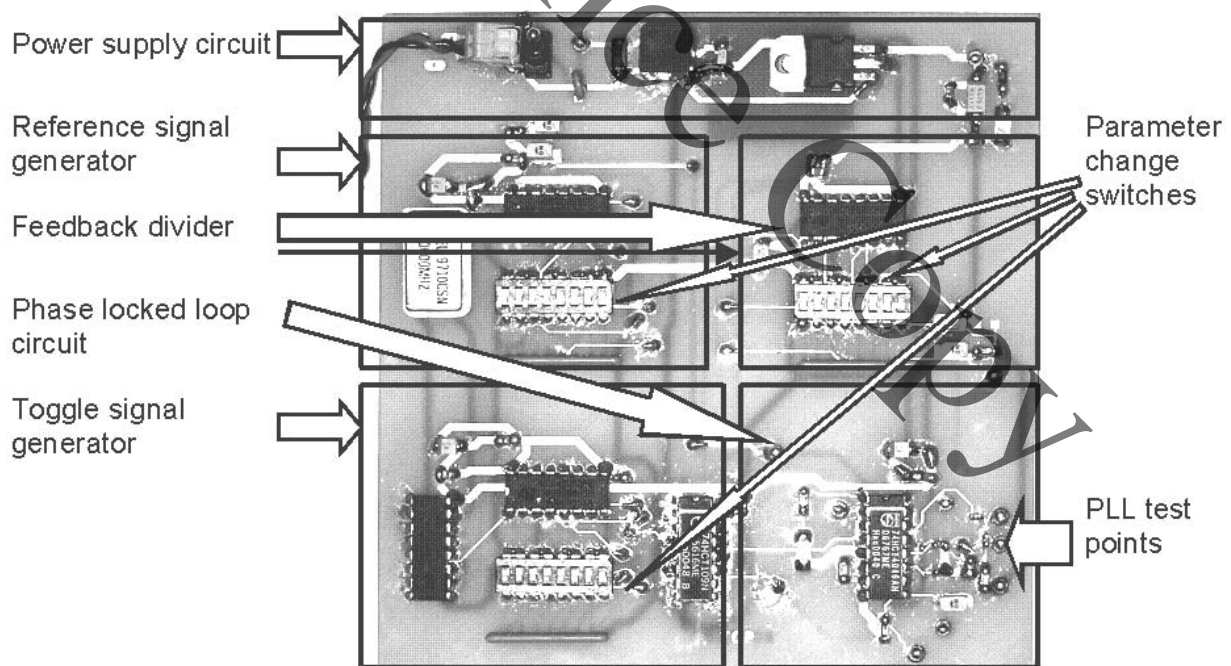
The cursor functions available within the simulation environment can be used to estimate the peak-to-peak output of the loop filter capacitor voltage and the time difference between the peak of the input signal and the peak of the loop filter response. The measured values can then be used to ascertain the peaking and phase delay of the output signal for the particular modulation frequency. The appropriate equations and methods are included in the associated lab session notes. A summary of the technique is also given in section 3.

To provide a suitable transient response settling time the measurements should be taken after the PLL has settled, i.e. after about 3.5ms in the plot. Using the simulation model it is possible to alter the input modulation frequency and make further measurements to produce plots of the phase transfer function similar to the ones illustrated in figure 2.

Material relating to other measurements follows the same general format as that shown. Further supplementary information relating to the measurements is provided in the course lab notes.

### 3. Experimental hardware details and examples.

The central part of the course material is the hardware demonstrator board. This board is based on a 74HCT7046<sup>14</sup> Phase locked loop integrated circuit. This circuit element comprises the core of the demonstrator board and the internal operation is the same as that explained in section 2. An illustration of the demonstrator board outlining key components is provided in figure 6.



**Figure 6** Circuit layout for hardware demonstrator board.

It can be seen from figure 6 that the physical PLL hardware board contains additional system elements to that shown in figure 1.

The key differences in the real circuitry are as follows: 1) Addition of power supply regulation circuitry; 2) Addition of an on board reference signal generator circuit. This circuit is analogous to the voltage source (V2) shown in figure 1; 3) Addition of toggle signal generator circuitry. This is used to generate appropriate step signals for the step response measurements.

Various switches and test points are also included on the circuit board. DIP (Dual Inline Package) switches are used to change the reference frequency, feedback division ratio, and the frequency step application frequency. In addition various single switches are used to facilitate connection of external test signals to the board. Test points are included to allow full monitoring of critical PLL signals, such as, reference, feedback, loop filter, and phase detector signals.

The hardware board can be reconfigured in a variety of ways to allow experimentation with various characterisation scenarios. Typical tests include step response, and transfer function response measurements. However, prior to carrying out these experimental measurements a complete lab session is devoted to basic functional checking of the hardware. In this stage components such as the main power supply, toggle circuitry, PLL circuitry, and reference circuitry are verified. A strong emphasis is placed upon the importance of this process as it ensures that each student has a correct starting point prior to carrying out more involved experiments. The session also assists as a refresher in oscilloscope based measurement techniques.

After the initial verification process has been carried out, all of the more advanced lab sessions follow a common format consisting of the following information: 1) General explanation of the specific measurement and the associated theory; 2) Initial board and measurement equipment set up detailing instrument settings and switch settings; 3) An initial example of the measurement procedure. Following execution and evaluation of the initial measurement example the students are asked to carry out various experiments that require modification of various system parameters. Analysis of these experiments is used in the final assessment. An example of a particular lab session relating to PLL transfer function measurement is now provided.

### 3.1. Example of PLL transfer function measurement; Motivations and theoretical background.

In this lab session the transfer function of a PLL system is measured. The results of the measurements are used to extract phase and magnitude response plots for the PLL. The transfer function of a PLL (or any real system) is important because it uniquely defines the operation of the system.

Initially the lab session notes provide an overview of transfer function measurement techniques relating to commonly encountered electrical or mechanical systems, such as RLC networks, mass spring damper systems, OP-amp filters etc. The course material provides detailed graphical and verbal examples explaining experimental transfer function measurement of a system with a voltage input and a voltage output. For this type of circuit

The magnitude information in dB at a particular frequency is generally found by:

$$\text{Magnitude} = |H(j\omega)|_{dB} = 20 \log_{10} \left( \frac{V_{out}}{V_{in}} \right) \quad (\text{db})$$

**Equation 12 Conventional dB Magnitude calculation**

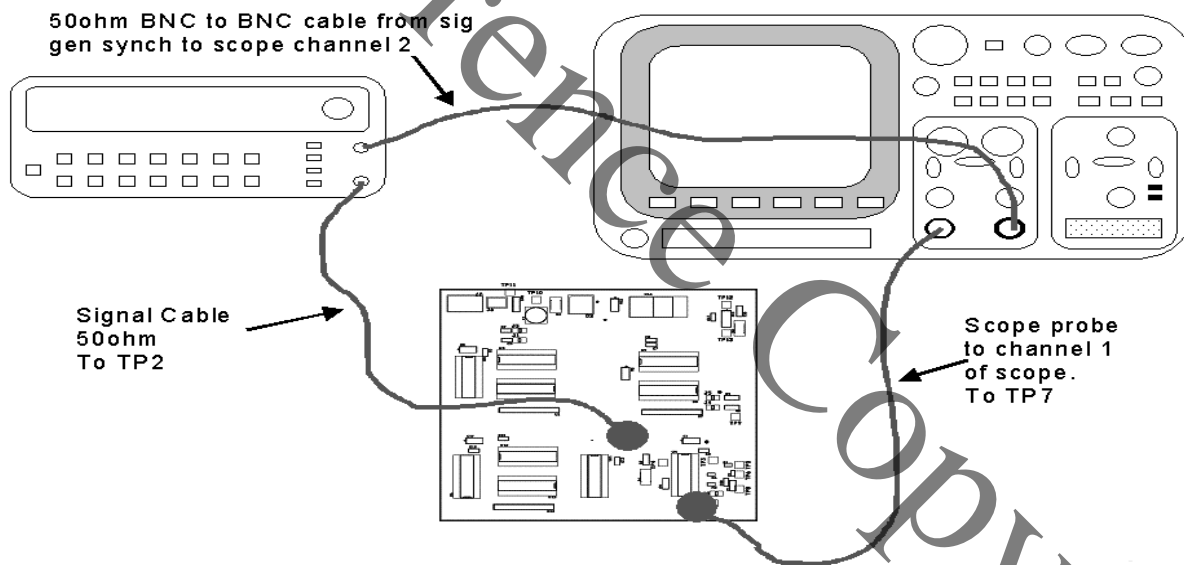
The phase information can be found experimentally by comparing the relative time difference between the zero crossings of the input and output waveform. Further details of this process are documented in the full course text.

For a PLL system it must be remembered that the input and output parameters are in terms of time varying phase and not time varying voltages, currents etc. So to carry out a transfer function measurement of a PLL a sinusoidally varying phase (or phase modulation) has to be applied as the input parameter, and the output response will be a sinusoidally varying phase. To simplify the generation of a real input signal it can be shown that for PLL systems a phase-modulated signal is equivalent to a controlled frequency modulated signal<sup>2</sup>

The result from equation 12 evaluated at different input frequencies can be used to construct a transfer function plot similar to that shown in figure 2.

### 3.2. Example of PLL transfer function measurement; Lab set up and response plotting.

In the initial stages of the measurement procedure, hardware switch settings relevant to the particular experiment are provided. The switch settings are fully documented in a tabular form and cross-referenced to a scaled block diagram of the hardware board layout. Following this the connection details for the measurement instruments are provided. Figure 7 shows an illustration used to aid explanation of the measurement set-up.



**Figure 7 Test Hardware Physical set-up.**

Viewed from left to right figure 7 shows the signal generator, hardware board, and oscilloscope connections.

Principle connection details are also documented in table 1.

Block#	Test Function	Schematic Designator
1	Allows an external reference signal from the signal generator to be applied to the PLL.	TP2 (see figure 7)
2	DEMODO output of PLL. Allows monitoring of the PLL loop filter node, without unduly loading the node.	TP7 (see figure 7)

**Table 1 Test pin function table.**

In table 1 Block # indicates block references used in the scaled block diagram mentioned previously. After the appropriate connections have been made and checked the student is led through an initial set-up procedure. This stage is included to ensure that the students all have a working evaluation system prior to performing further experimentation.

Examples of typical measurement instructions are provided below.

Throughout the exercises the measured results are imported into an Excel™ spreadsheet. The Excel spreadsheet includes equations to automatically plot the transfer function response. The import procedure is carried out using Agilent Intuilink 54600 Excel™ toolbar.

### Measurement Control Details:

The following instrument settings are used to make the phase transfer measurement.

- 1) Adjustment of modulation frequency. The modulation can be adjusted by using the following signal generator buttons. *Shift => Freq => adjust the control dial until the required modulation frequency is set. Note that the <> arrow keys can be used to alter the control dial resolution.*
- 2) Note that for higher modulation frequencies the trigger level control of the oscilloscope may have to be adjusted until the correct response is achieved.

### Response Analyses Capture:

By changing the modulation frequency (see above) the PLL transfer function is measured in the following manner.

- 1) Set modulation frequency 100Hz \* # and use the cursors to measure the following parameters.
  - a. Peak to Peak output voltage of the loop filter output.
  - b. The time difference between the null of the loop filter output and the signal generators synchronisation pulse.
- 2) Record the values from 1 in the appropriate locations in the Excel™ spreadsheet.
- 3) Increment # and carry out measurements until it is difficult to monitor the loop filter output signal.

In the above process the first measurement is taken as a datum measurement. Justification of this statement is provided in the full course notes. Using this feature allows magnitude measurements to be made with respect to an initial measurement. So equation 12 can be modified as follows:

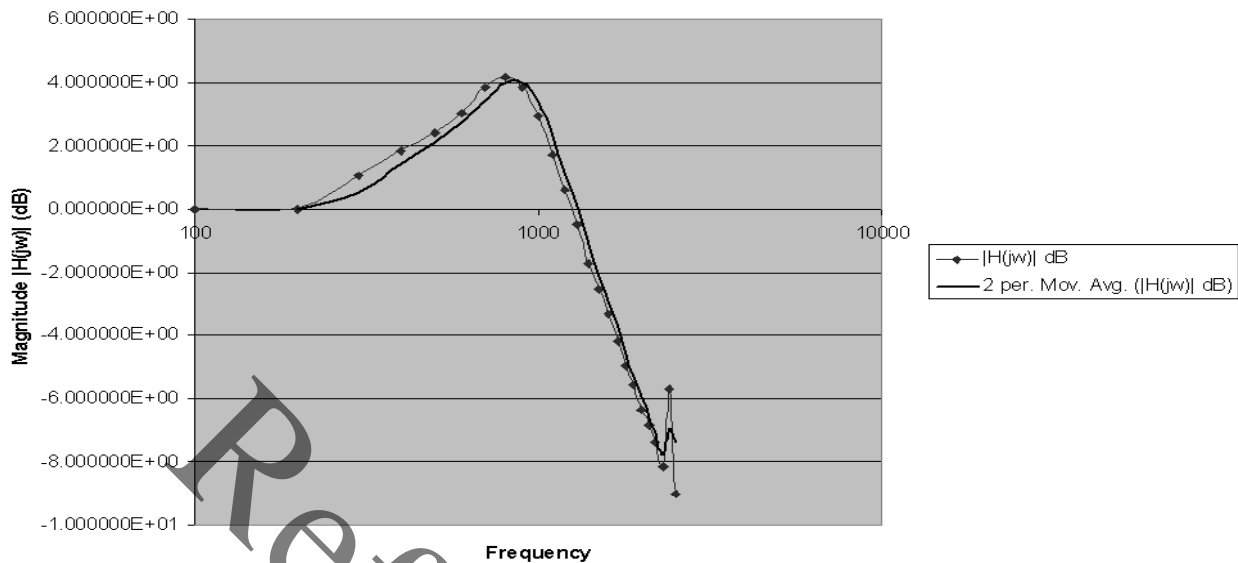
$$|H(j\omega)dB| = 20 \log_{10} \frac{Vm_{100Hz}}{Vm_N} \quad (\text{dB})$$

#### Equation 13 Modified PLL specific magnitude calculation.

Where  $Vm_{100Hz}$  is the peak-to-peak voltage measured at an input modulation frequency of 100Hz and  $Vm_N$  is the Nth peak to peak voltage output for a corresponding input modulation frequency.

### 3.3. Response plotting and example assessment questions.

After carrying out the exercise a magnitude response plot similar to the one shown in figure 8 Should be produced.



**Figure 8 Example response plot for the PLL transfer function measurement.**

After plotting the phase and magnitude graphs the student is asked to print them out with indications of where the appropriate PLL parameters can be determined. The graphs should be handed in as part of the assessment procedure. The student is also asked to compare the hardware results with simulated results. In addition to plotting of the response curves, various questions relating to the transfer function response and measurement procedure are asked. Initial questions relate to the estimation of the natural frequency, damping factor and 3dB bandwidth of the loop directly from the response plots. In all of the lab sessions the student is encouraged to carry out further investigation into the system operation. For the transfer function measurement the student is asked to change the system design parameters, produce a new transfer function plot, and comment on the change in system behaviour.

#### 4. Conclusions and further work.

This paper has outlined a set of practical and theoretical course material related to the measurement and design of Phase locked loop systems. Primary focus of the material is towards characterisation, measurement and design of a real demonstrator circuit. However, a significant theoretical and simulation based aspect of the course is included. Simulation models used map to the physical hardware system and allow the student to experiment with various measurement scenarios prior to attendance of the lab sessions. Throughout the material emphasis is placed on observing differences between real and simulated measurements. Although material is related specifically to phase locked loop systems, techniques used and information given are also of benefit in reinforcing general control and feedback theory. The general teaching approach of coupling specific simulation models with hardware demonstration boards has received promising student feedback.

#### Acknowledgement

ILSI Livingston, Scotland for providing resources and support.

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