Detection and Evaluation of Deterministic Jitter Causes in CP-PLL's due to macro level faults and Pre-Detection Using Simple Methods

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Abstract

Charge-Pump Phase-locked loops are currently used in a variety of signal generation applications. Due to the usefulness of the device CP-PLLs are now commonplace inclusions in SOC designs, and ultimately determine performance of other SOC blocks, such as ADC's, DAC's, RF functions and fibre communications channels. In many situations, only simple frequency lock tests are carried out on the PLL portion of a circuit, with other complex direct jitter tests being indirectly carried out at a higher system level. Although these higher level system tests must generally be carried out at some point they can be time consuming, in addition, if the PLL is designed and operating correctly the PLL system will generally have a far better performance than the system it is driving. This paper investigates typical jitter output responses of CP-PLLs when subjected to selected forward path faults, particularly relating to forward path leakage effects in the main integration capacitor. The evaluation platform consists of a macro level mixed signal based PLL-Model. Degradation of the PLL outputs are evaluated from the phase noise spectrum and jitter spectrums and sideband spur degradation. Further evaluations and analysis are supplied relating block level effects to jitter and investigations are made as to the efficacy of detection of these errors with simple measurement techniques. The crux of the work is thus initially to develop techniques to aid evaluation of the likely jitter performance of a PLL system without resorting to direct measurement techniques.

Keywords: PLL, CP-PLL, Jitter, Deterministic Jitter

1. Introduction

Charge-Pump Phase-locked loops (Charge-Pump Phase-locked loops) are currently used in a variety of situations, including on chip clock synthesis, RF carrier synthesis, and modulation and demodulation applications. Due to the usefulness of the device, CP-PLLs [1] [2] [3] [4] are now commonplace inclusions in SOC (System on Chip) designs, and often ultimately determine performance of other SOC blocks, such as ADC's, DAC's, and fibre communications channels. CP-PLLs are often evaluated in the design and characterisation phase of product development in terms of the transient response and transfer function response. Results from these evaluations will give an indication of the expected performance of the PLL in terms of phase noise output (or jitter output). In addition to the typical response measurements, direct jitter and phase noise measurements generally accompany design characterisation in both the simulated and real environments. In the production test phase, often it is assumed that the PLL performance is "right by design" or "guaranteed by design" and that the intrinsic noise filtering characteristics of the PLL will ensure a device with adequate performance. Examples of typical PLL analysis procedures can be found in [4][5][6]. The "right by design" assumption is valid for a perfect design with component variations within the process limits, however it does not hold in the presence of faults. During the design phase much effort goes into minimising the effect of noise introduced into the loop from external sources and maximising the natural noise suppression of the loop. Typical design methods for PLL noise suppression relate to low noise oscillator design, maximizing the loop bandwidth and efficient supply decoupling methods for the whole PLL and VCO (Voltage Controlled Oscillator). VCO's can be very sensitive to external coupled noise form supply rails or via the substrate and this coupling mechanisms can lead to direct modulation of the VCO output signal. In many instances PLL cores situated on chip have their own separate power supply lines and utilise techniques

such as local on chip decoupling capacitors and bond wire LC filters in the attempt to desensitize the loop components to externally induced noise [7][8][9][10].

Although, as mentioned, extensive characterisation is generally used in the design and development phase of the PLL prior to production, tests on the PLL are sometimes radically reduced in the production test environment. Test reduction can occur due to many factors such as time scales, access problems, and test integration. Some key issues are outlined in [11].

In many situations only simple frequency lock tests are carried out on the PLL portion of a circuit, with other complex direct jitter tests being indirectly carried out at a higher system level. In the frequency lock test the PLL systems output signal frequency is simply measured a certain time after start-up (or after a defined change in input frequency) to see if it is at the correct operating frequency or phase. As frequency counting performs an averaging operation it can be difficult to monitor short-term variations in the output signal. In fact it is shown in [12] and later in this paper that in many instances the PLL will still have the same average output frequency for output signals with vastly differing short-term instantaneous frequency deviations.

Indirect measurements are often carried out at the higher system level and will depend upon the final system application. These may include measurements of ADC noise (where the ADC is clocked by the PLL) or symbol synchronisation measurements (such as eye diagram measurements) of a data stream that is ultimately dependant on the PLL clock. Although these higher level system tests must be carried out at some point (unless the system is found to fail a-priori) they can be time consuming, in addition, if the PLL is operating correctly and the "right by design" assumption is made, the PLL system can have a far better system performance than the system it is driving. For example jitter due to ISI (Inter Symbol Interference) in a communication channel could mask any jitter present from a correctly designed and error free PLL system. If however, the PLL system is faulty the reduced performance will propagate to the higher-level system function performance, thus leading to system degradation.

Typical faults in the CP-PLL may include charge pump errors, loop filter errors, oscillator sensitivity to coupling noise and mismatched phase frequency detector paths. [4] [13][14][15][16]Many of these errors can be highlighted using simple measurement techniques [12] and it seems sensible to carry out this type of test prior to more elaborate higher-level system function tests. The focus of this work is thus to attempt to rapidly isolate faulty components before investing time in more complex and time-consuming tests. In addition, for a PLL operating under typical noisy conditions, the jitter induced from leakage effects should be much greater than the expected jitter contribution from the oscillator. Furthermore, in many instances it is possible that measurement of CP-PLL forward path deviation in conjunction with oscillator power supply rejection ration tests will be adequate to determine system performance.

The primary focus of this paper is towards jitter relationships and phase noise spectrum degradation due to loop filter leakage from the main loop filter capacitor. Other forward path effects are considered briefly. This component is initially chosen because of potential sensitivity to process defects and its critical function in PLL operation. In embedded applications, the loop filter component is constructed from a very large (approx 100 pF) MOS capacitor structure. Also, leakage due to this component can cause analogous affects to excessive charge pump mismatches or forward path delay faults. However, it is expected that the magnitude and likelihood of performance degradation due to typical errors in the loop filter capacitor will generally be much greater. Effects from forward path errors can be highlighted using simple techniques [12] and if required, contributions due to various effects can be decomposed using techniques shown in [12] and also mentioned later.

It must be mentioned at this stage that various excellent papers also exist relating to BIST (Built In Self Test), DfT (Design for Test) techniques for evaluation of various PLL parameters [17][18][19][20][21][22]. In addition, various papers are in existence concerning behavioural modelling techniques and fault evaluation techniques for CP-PLL's [23][24][25][26][27]. Furthermore various researchers have looked at practical implementations of direct on chip jitter or precise timing measurement systems [28][29][30][31] 32][33][34][35] some of which are included with the overall PLL BIST solution. [17] . On chip solutions for precise timing measurements generally relate to adaptation of conventional off chip techniques such as, strobe based delay line, capacitor based linear interpolation, vernier interpolation measurements [36] and oscillator-based measurements to on chip implimentations. The main problem with the techniques is that they usually require analogue tuning techniques and occupy a large die area with respect to the SUT (System Under Test). This situation would not be as much of an issue if the test resources could be shared amongst several SUT blocks or measurement points. In fact techniques suggesting multiple probe locations with one measurement unit are under investigation in [34]. However, it is debatable whether accurate repeatable timing measurements of high frequency signals will be possible in the presence of system noise and different interconnect delays. In addition, it may be difficult to justify inclusion of extra high frequency interconnects into an overall system design. However, with reducing device size, increasing on chip and on

board system frequencies and associated problems with physical interconnects the probable advent of new wireless interconnect schemes [37] may make on-chip direct jitter measurement schemes a viable alternative for the evaluation of the master transmitting modules.

Although various papers have been mentioned relating with respect to PLL measurement / jitter measurement and the associated modelling issues, test techniques outlined in [11] and [12] were initially devised to allow desensitization of the PLL loop, to facilitate monitoring and decomposition of key jitter contributors using very simple techniques. Initial input stimuli sequences to achieve decomposition were outlined in [12] along with qualitative observations of loop filter leakage and jitter degradation. These observations are also extended in [38 My IMSTW03] and this paper to initially relate open loop leakage effects to likely closed loop jitter or phase noise performance. It is the intention that the open loop deviation tests for the PLL forward paths will be accompanied by an open loop measurement of the VCO using simplified direct measurement circuitry. To assess noise immunity the VCO measurements will be carried out in a clean and noisy environment (e.g. with on chip digital circuitry active and inactive) and in conjunction with deterministic noise injection circuitry. The ultimate crux of the work is to attempt to reverse the problem of jitter / phase noise measurement for CP-PLL's. That is, instead of using direct measurements on the PLL output, methods are sought that ease detection of the major phase noise contributors. In addition resultant circuitry should be simple and of low area so as to allow it to be included as part of every critical CP-PLL based core. This comment is of particular validity when considering the very likely advent of wireless interconnects schemes where each clock domain would require its own Phase locked loop based synchronisation circuitry. In consequence it is felt that with ever-increasing clock frequencies, component densities and the emergence of new interconnect proposals, that this approach may be the only viable method for high volume production test applications. To the authors knowledge the method of devising simple procedures suitable for low overhead on chip implementation that are specifically targeted with the intention of evaluating expected jitter and phase noise performance is a wholly new concept.

For the paper behavioural macro-level simulation models are used for the analyses, and the models are known to correlate well with representative physical hardware measurements. The behavioural models were evaluated using design parameter values such as charge pump current and VCO gain taken from a number of fully designed Integer N CP-PLL cores. Simulated results were then compared to real measured results. Typical evaluation measurements related to start-up response, step response and observation of the output spectrum or phase noise response.

The models allow provision for injection of random noise and deterministic noise into various sections of the PLL, with the prime intention of highlighting the generally much greater effect of forward path leakage effects.

The paper is broken down into the following sections Section 2 explains the macro level models used and the assumptions made for the initial experimental work. It also identifies locations and techniques for macro level fault injection. Typical macro level faults include loop filter leakage, CP (Charge Pump) mismatch, oscillator sensitivity or noise, and delay faults in the PFD (Phase frequency detector).

Section 3 is used to explain and identify techniques for investigation of the phase noise spectrum and jitter spectrum. It also describes techniques used for generation of the jitter spectrum using a SPICE simulator and MATLAB routines.

Section 4 Initially investigates typical jitter and phase noise output responses from the faulty PLL and evaluates the efficacy of detection with simple open loop leakage tests. This leads to a relation ship between constant phase offset and open loop frequency deviation. In addition this section relates the constant phase offset back to the likely deviation of the loop filter control voltage.

Section 5 provides a summary and conclusion of the paper and gives indications as to where further work is required.

2. Macro level CP-PLL model.

Figure1 Illustrates the block level diagram for the PLL macro model

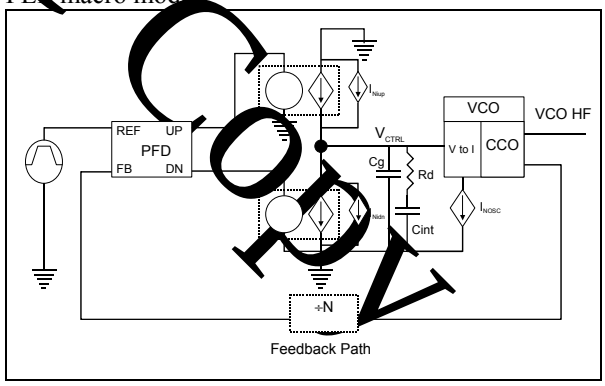

Figure 1 Key elements of PLL macro model.

The key elements of the model are now described from left to right with associated methods for fault inclusion.

The reference signal for the PLL is currently modelled using a conventional SPICE pulse source. For the analyses it is assumed that a clean reference source is available.

The PFD (Phase Frequency Detector) is modelled as an edge sensitive type IV phase and frequency detector

and is described using VHDL primitives consisting of two D-type flip-flops an AND gate and various inverter delays. Each primitive in the PFD can have its associated propagation delay (which relates to the dead band of the PFD) changed using generic parameters available in the VHDL language.

The charge pump sources are modelled using voltage controlled current sources. The model has also been evaluated using MOS switches. The model has associated current sources I_{Nup} and I_{Ndn} that can be used to model the effects of noise in the charge pump structures. However, for the particular analyses it was assumed that any noise modulation effects could be combined with the VCO noise modulation.

The loop filter components are standard SPICE elements. C_g is the decoupling capacitor that removes high frequency transients from the charge pump switching action. R_d is the loop filter-damping resistor. C_{int} is the main loop filter capacitor.

The VCO is modelled using C like constructs included as part of the simulation package. The VCO model incorporates the division ratio of the PLL system (included in frequency synthesizers) and the divided signal is fed to the feedback path input of the PFD. The VCO also has a high frequency output i.e. the real output of the PLL that is mapped to the feedback output. For the initial modelling it is assumed that the forward path low frequency section of the PLL, consisting of the PFD, CP and loop filter respectively, will be identical whether the PLL's final output is high or low frequency. That is, changing the division ratio can change the PLL's ouput frequency range, whilst the VCO gain, CP gain PFD delays and loop filter components can be adjusted to keep the loop filter parameters approximately constant. [38]

To allow correct noise to be injected into the VCO, various assumptions are made for selection of typical target architecture. The primary assumptions are that the delay cells in the oscillator will be differential current starved elements, and the control voltage (V_{ctrl}) from the loop filter will steer the oscillation frequency via a voltage to current conversion stage. It is also assumed, following [39], that for this architecture the primary source of direct oscillator induced jitter (random or deterministic) will be due to modulation of the tail current. The block diagram of the VCO tail current noise model is shown in figure 2.

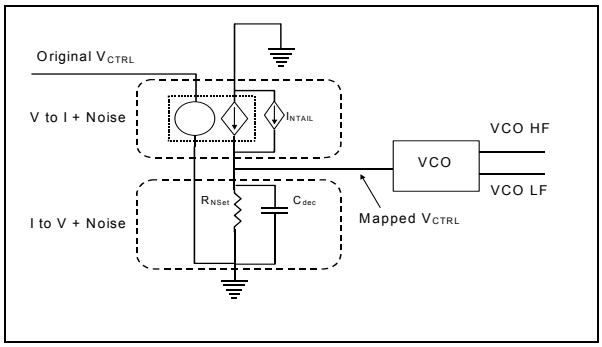

Figure 2 Controlled Oscillator Noise Injection model

As can be seen from figure 2 the model is decomposed into 3 basic sections. The V to I conversion allows a random or deterministic noise current to be injected. The I to V section includes a noise model resistor (that includes thermal and flicker noise effects) and a decoupling resistor C_{dec} which is used to model the supply decoupling. C_{dec} also effectively slew rate limits the VCO frequency change at high input frequencies.

To assess the accuracy of the noise model a 2nA 10MHz sinusoidal noise current signal was injected into the oscillator. This experiment was also carried out in [39] and the phase spectrum plot in figure 3 illustrates comparable results, with the spurs due to the 2nA noise modulation clearly evident at a 10 MHZ offset.

The simulations carried out in subsequent sections of this paper are carried out with random noise of 2nA amplitude injected into the oscillator cell. The model has been described and simulated in the SMASH™ simulation environment. Further evaluations, including extractions of propagation delays, have been carried out and compared in Agilent Technologies ADS simulation package [40].

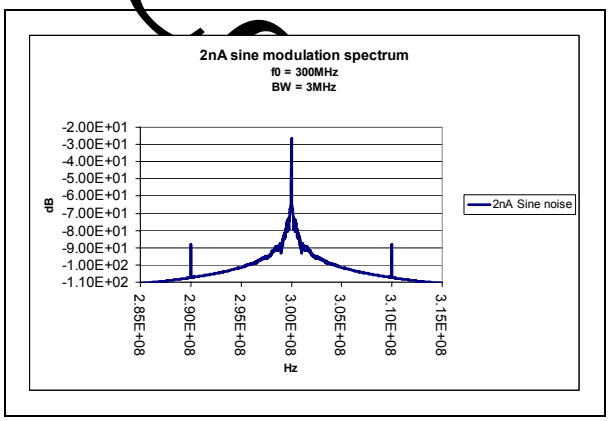

Figure 3 Oscillator spectrum with 2nA sinusoidal noise modulation

The specific parameters and derived parameters relating to the model are provided in table 1, in addition noise parameters and error parameters are given.

Design Parameters	Comments	Value
Ref	Reference Frequency	10 MHz
Division Ratio	Feedback divider ratio.	30
Desired Output Frequency	Final PLL output frequency.	300 MHz
Ipump	Charge pump current magnitude	10 uA
PFD delay	Propagation delay in one path	700 ps
Kvco	VCO gain MHz/V	200 MHz /V
Ivco	VCO gain MHz/uA	2MHz / uA
Vctrl Range	Tuning voltage range.	1 to 2V
Ictrl Range	Tuning current range.	100 to 200 uA
Cint	Main loop capacitor.	100 pF
Cg	Deglitching capacitor.	10 pF
Rd	Damping resistor.	25 Kohm
Derived Parameters		
ω_n	Natural Frequency	816.496 Krps 129.949 KHz
ζ	Damping Factor	1
B_L	Noise bandwidth (one sided)	510 Krps 1.2183 KHz
Noise Parameters		
I_{NOSC}	Random noise modulation of oscillator	2nA peak
I_{NPUMP}	As above for charge pumps	2nA peak
Errors		
R_{LEAK}	Loop filter leakage resistor	100M, 10M, 1M, 100K, 10K (ohm)
ΔI_{updn}	Change in charge pump current magnitude.	±20%
ΔPFD	Delay change in PFD	±10%

Table 1 Model parameters.

Equations for derived parameters can be found in [1][2] [3] [6]. In addition, operational details of the various elements can be found in the same references. Any key equations and operation details required for this paper are provided where applicable.

The critical design parameters were estimated from a selection of representative PLL designs constructed in contemporary technologies.

Simulations for the model for typical evaluations including, start-up response, step response, phase transfer function, phase noise and jitter performance, bare a close correlation to actual measured results.

Typical fault / error injection at the macro level is related to CP mismatches, loop filter leakage, PFD delay mismatches and VCO modulation leading to output frequency modulation by these effects. The main focus of the work at present is related to the investigation of deterministic phase noise at the output due to these types of faults and is principally related to direct loop filter leakage. Experiments for this model have been carried out with further errors in suggested components, however, the most dominant effect appears to occur from typical loop filter errors.

It is noted that cumulative drift of the PLL output frequency due to any leakage or delay in the forward path components can be mapped in the first order to biasing of the loop filter control voltage. For further analysis however; the following faults can be applied.

Delay faults in the PFD are introduced by adjusting the propagation delays of the associated VHDL models. Mismatch faults in the CP structures can be introduced by changing the gain factors of the VCCS (voltage controlled current source). Leakage effects in the loop filter structures are introduced by placing resistances in parallel with the relevant loop filter capacitor.

3. Generation and analysis of the jitter spectrum.

This section investigates techniques for generation of the jitter output spectrum from the PLL model. The jitter spectrum model is used to provide a visual indication of the induced jitter when the PLL subjected to likely errors in the loop filter components.

The basic method for generating the jitter spectrum from a SPICE simulation involved subtracting an "ideal" reference signal from the PLL generated signal to generate a TIE (Time Interval Error) output signal. This signal contains pulses whose amplitude represents the time difference between the respective signals. An algorithm to plot the time interval error with respect to time was developed for the SMASH™ simulator in the ACD behavioural modelling language. Further measurements were also taken from models created for the Agilent ADS simulation package using the cross() function. The algorithm detects occurrences of the rising edges of the two signals and stores the respective simulation step times in local variables. When two rising edges have been detected the associated occurrence times are subtracted to yield the TIE. The value is then output to the simulator display and the local variables are cleared for the next measurement. The algorithm has also been mapped to the VHDL-AMS language.

Applying an FFT to the discrete TIE output signal yields the jitter output spectrum. This spectrum can be analysed and post processed to determine and separate random jitter and deterministic jitter [41][42]. In general, deterministic jitter will be seen as discrete spectral lines in the jitter output spectrum, whereas random jitter will be observed as a "noise" floor at some constant amplitude. For the purpose of the paper the jitter power spectrum is produced in SMASH and conversion to the appropriate jitter versus frequency plot is carried out via post processing in MATLAB and EXCEL.

For reference, figures 4 and 5 show the time interval error plots and peak-to-peak jitter spectrum plots respectively. These plots were taken from the closed loop PLL model.
The result plots illustrate the PLL jitter response for different input currents injected into the VCO. The measurements were carried out over 15000 PLL output cycles with the oscillator subjected to 200nA peak amplitude sinusoidal current noise at modulation frequencies of 100 KHz and 1 MHz.
The 200nA current value was chosen as an example in this case to allow easier viewing of the response plots. The responses were also plotted with 2nA-injected noise current as mentioned in section 1. However, with this value of noise the change in the PLL output response was negligible with the deterministic spike shown in figure 5 being buried in the noise floor.

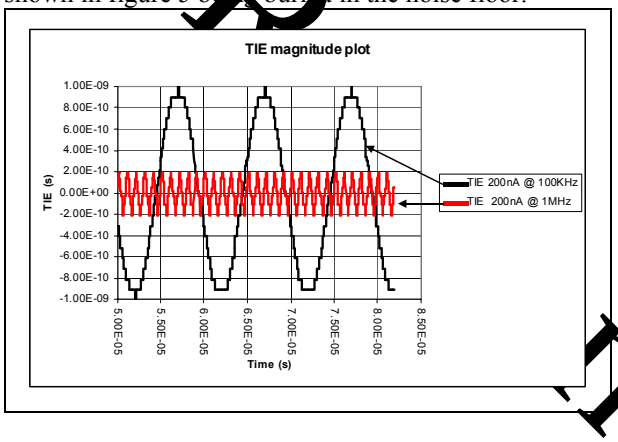

Figure 4 Time interval error plots for 200nA sine modulation @ 100KHz and 1MHz.

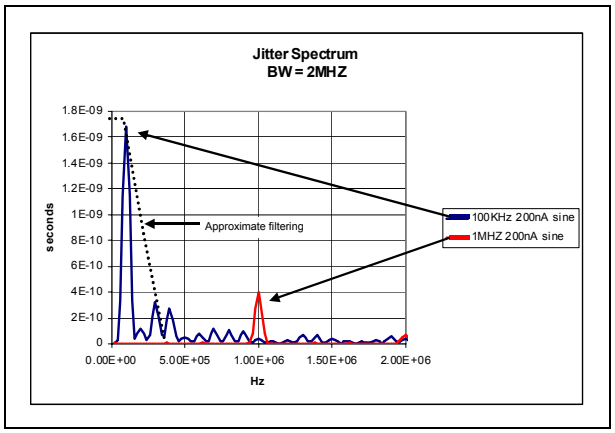

Figure 5 Jitter spectrum for 200nA sine modulation.

It can be seen from figures 4 and 5 that the peak-to-peak jitter magnitude of the jitter spectrum corresponds to the peak-to-peak magnitude of the TIE plot. It is important to note the jitter suppression of the 1MHz sinusoidal noise is due to the filtering function of the PLL loop filter. With reference to table 1 it can be seen that the 1MHz signal is outside of the estimated PLL noise bandwidth. The jitter spectrum view of output noise was found useful for qualitative observations of deterministic degradation of the PLL output spectrum.

4. Jitter output spectrum / Phase noise spectrum results due to loop filter errors and simple detection of faults.

This section initially investigates the jitter output spectrums and the phase noise spectrums of the PLL after injection of faults into the loop filter capacitor. The section then investigates detection of the performance degradation using simple techniques proposed in [12].

4.1. Principle investigations of phase noise degradation using conventional methods

Principle faults were related to leakage of the main integration capacitor (C_{int} , figure 1). As mentioned in section 1, the leakage effects were modelled by placing a resistor in parallel with C_{int}. This model is valid for MOS transistors used in a capacitor configuration. It was initially decided to concentrate on this element due to various factors, the principle being related to sensitivity to faults because of the large physical area, the critical relationship to overall PLL operation and the possibility of emulating other fault types with this approach.
Initial values for the leakage resistance were chosen as in table 2.

Leakage Resistance Value (R_{leak})	PLL centre frequency
100 M ohm	300 MHz
10 M ohm	300 MHz
1 M ohm	300 MHz
100 K ohm (not valid)	200 MHz
10 K ohm (not valid)	200 MHz

Table 2 Leakage resistances.

The 100 K and 10 K values are indicated as not valid due to the fact that with these leakage values the centre frequency of the operational PLL is shifted dramatically from the correct frequency. For these conditions the leakage resistance is so excessive that PLL circuitry can no longer compensate for the leakage per comparison cycle. That is it cannot maintain the desired average control voltage to keep the PLL output signal at the desired average frequency. In this situation the control voltage then settles at its minimum value. This effect makes it difficult to compare the output results with the ideal case, however the conditions would be easily detected by simple evaluation techniques such as a frequency lock test. It is important to note that this effect is the same as that reported in [12] from measurements carried out on physical hardware.

Plots are now shown for the full phase noise spectrum, the one sided spectrum and the jitter spectrum, respectively. For reasons of clarity, only the no leakage case and the case for R_{leak} = 1 MΩ are shown, however, tabulations of estimated phase offset and jitter for the other values are provided in tables 3 and 4. The other graphs, if shown would lie between the illustrated plots in figure 6 and 7.

The plot of figure 6 shows the full phase noise spectrum of the PLL output over a 40 MHz bandwidth.

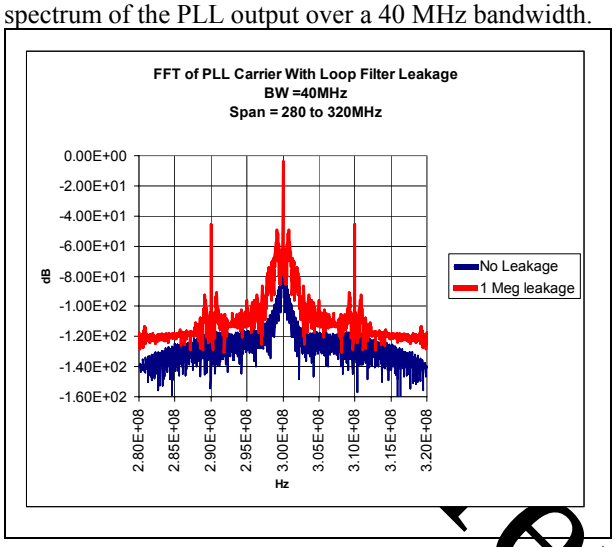

Figure 6 Phase spectrum plots for R_{leak} = ∞ (lowest plot) and R_{leak} = 1 M Ω

From figure 6 the degradation in the carrier spectrum can be clearly seen. There is also a degradation in the reference spur of approximately 50dB at a 10 MHz offset.

Plots of figure 7 are used to illustrate the one sided spectrum for the PLL output over a 10 MHz bandwidth. The plots of figure 7 were also used to estimate the phase jitter values in table 3.

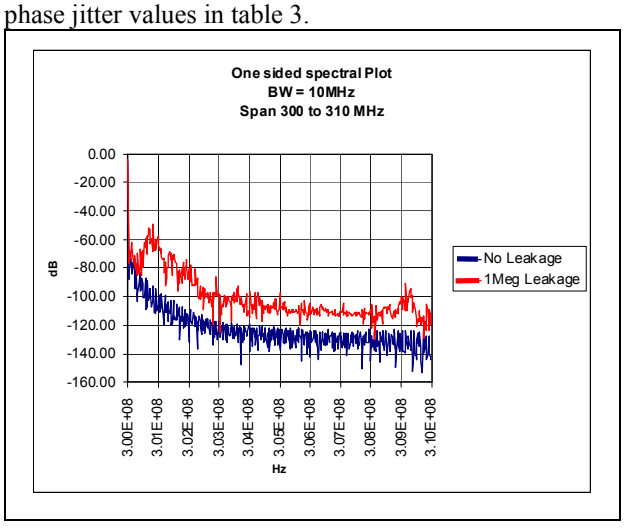

Figure 7 One sided spectral plots for R_{leak} = ∞ and R_{leak} = 1 M Ω

Figure 8 illustrates the jitter spectrum for the two leakage resistance cases over a 10 MHz bandwidth.

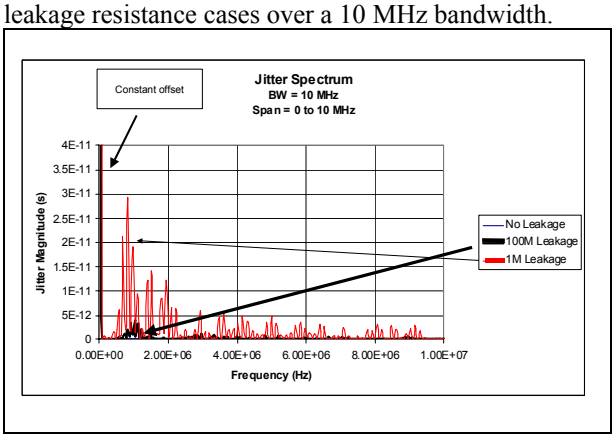

Figure 8 Jitter Spectrum for R_{leak} = ∞ , R_{leak} = 100 M Ω , and R_{leak} = 1 M Ω.

In figure 8 the jitter spectrum for R_{leak} = 100 MΩ, is shown for reference.

It must be mentioned that a constant offset (or static phase error) is evident in the jitter spectrum of figure 8. This offset occurs for the simulations with leakage resistance included, and occurs due to the phase that is lost per comparison cycle. The offset is easily seen from investigation of the TIE values and the associated jitter spectrum; however, it is not as readily evident from the phase noise spectrums of figure 6 and 7. The offsets were also calculated from averaging the time interval error and were also compared to measurements taken between the PLLs reference and feedback signal timing edges. The values are provided in table 3.

R_{Leak} (Ω)	Constant offset	
	Measured	TIE (average)
100 MΩ	153 ps	150 ps
10 MΩ	1.7 ns	1.5ns
1 MΩ	14.52 ns	14.6 ns

Table 3 Peak offset values.

The significance of this constant offset value is that the closed loop CP-PLL will always try to compensate for it per comparison cycle. This will lead to direct modulation of the VCO control as shown in section 4.4.

It can also be noted from comparison of figures 7 and 8 that a rise occurs at 1 MHz from the carrier. This peak is due to additional low frequency modulation of the VCO by the control voltage signal. Figure 7 was used to provide estimates of the RMS phase noise and jitter within a 10MHz bandwidth for the respective leakage values. From [2] the phase jitter estimate is made by integration of

L(fm) (see figure 7)

Where L(fm) is defined as the one sided phase noise spectrum of the signal .

Over the respective frequency range of interest. The process and associated variations are explained in [2] and the initial estimations were made using the associated software supplied in [2].

For comparison, RMS jitter estimates were also taken from the standard deviation of the of the respective TIE data. The standard deviation was taken so as to remove the significant constant offset jitter. Note that for deterministic jitter sources RMS measurements are not wholly applicable, however in this situation they serve to provide an indication of the noise degradation over a specific bandwidth with increasing leakage resistance values.

Table 4 indicates estimated values for timing jitter within a 10 MHz bandwidth. The values were also compared with the standard deviation of the time interval error plots and gave results within a similar range.

R_{leak}	TIE est (ps)	Phase est (ps)
∞	163	11.06773
100 M Ω	98.7	121.2082
10 M Ω	392	434.0493
1 M Ω	638	794.0122

Table 4 Estimated Jitter values for various leakage resistors.

From the estimations in table 4 it can be seen that if the maximum timing deviation is to be no more than 10% (commonly stated performance metric) of the required signal frequency that is

$$T_{Jitter} \leq T_c \bullet 0.1 \qquad \text{(seconds)}$$

Equation 1

Where T_c is the period of the required signal

The last two conditions in table 4 will have produced unacceptable system degradation. It is possible that in many situations that jitter degradation for the 100 M Ω resistance case would also be classified as leading to unacceptable system performance.

Obviously the jitter specification or phase noise specification and the measurement bandwidth will depend ultimately on the final system application. However, the tabulated measurements give a useful indication of performance degradation. Also in many situations the constant offset will be of prime importance.

4.2. Detection of faults leading to jitter degradation using simple methods.

This subsection essentially concentrates on detection of the faults related to loop filter leakage explained in the previous subsection using simple techniques. These results are then related back to approximate peak offset jitter values. Techniques are based upon "Ramp stimulus" techniques, which are well documented in [12].

The basic principle of the technique is to open the PLL loop after lock has been achieved and then apply deterministic signals derived from the reference signal to the inputs of the PLLs PFD.

Before proceeding, with further explanation, a brief verbal description of the basic PLL operation will be given. Further more detailed descriptions are provided in [2][3].

In a locked condition the PFD serves to provide error correction pulses that are proportional to the timing differences between the reference clock and the feedback clock. The pulses are then used to switch the appropriate charge pump switches and ultimately raise or lower the loop filter control voltage (V_{CTRL}) accordingly. Noting that V_{CTRL} provides the VCO control signal, and in turn the VCOs output signal is fed back to the PFD input, it can be seen that in the locked condition the PLL will maintain an average output signal that is phase and frequency locked to the reference signal. Furthermore, assuming that the loop filter components are free from errors, and the oscillator is low noise and sufficiently decoupled, the PLL will maintain a very close average (i.e. low noise) to the clean reference signal. In this case the "dead band" or the limit at which the PFD can no longer detect a phase difference, will ultimately limit the maximum peak-to-peak jitter of the PLLs output signal. This assumption, however, is not valid if any of the forward path components are leaking at an excessive rate.

Now returning to the discussion of suitable stimulus application to the PFD inputs when the PLL loop is open and after lock has been achieved. It was demonstrated in [12] that application of identical signals to the PFD could be used to emulate the locked condition. Furthermore, it was shown the technique can also reveal leakage in the forward path of the PLL by measuring the output frequency deviation over a number of cycles of the PLL reference waveform. Note that it is suggested in [12] that the input signal is applied by use of an appropriately designed input multiplexer. The deviation is measured with respect to a start frequency that is measured when the PLL is operating in the locked condition. The output frequency deviation in the emulated lock mode is proportional to the leakage rate per PFD comparison cycle. In addition, it gives a direct indication of the amount of leakage per cycle when the PLL is in its fully operational locked mode. Graphical descriptions of the initial test set-up and a sketch of the PLL output response are shown in figure 8.

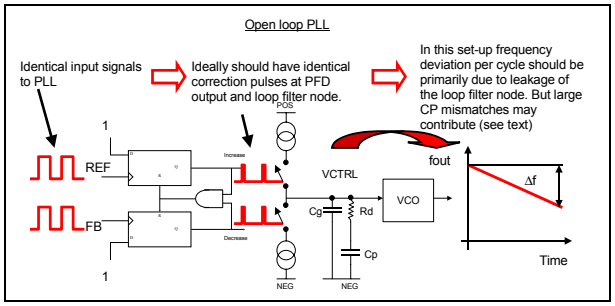

Figure 8 Suggested leakage measurement set-up

The technique shown in figure 8 and other permutations of the technique have also been evaluated using physical hardware platforms.

4.3. Initial measurement analysis of static offset procedure using "simple methods"

For the maximum offset error estimations taken from loop filter leakage plots, the assumption is initially made that the deviation over many cycles of the reference signal will be on average equivalent to the sum of the leakage over 1 cycle in the locked mode. In addition it as assumed that C_g (see figure 1) initially will have negligible affect on approximations, due to the small size of C_g compared to C_{int} this is a valid assumption and provides an initial starting point for calculations. Thus, measuring the deviation over multiple cycles and dividing by the number of cycles yields the approximate deviation per cycle.

$$\Delta f_{Cycle} \approx \frac{\Delta f}{N_{Cycles}} \qquad \text{(Hz)}$$

Equation 2

Where, Δf_{cycle} is the approximate deviation per cycle, Δf is the deviation over multiple cycles of the reference signal and N_{cycles} is the number of cycles the measurement is taken over.

The relationship in equation 2 has to be expressed in terms of time to give an indication of the maximum phase alignment the PLL attempts to compensate for during each comparison cycle. To accomplish this the initial assumption is made that if the PLL can maintain the required average frequency in the locked condition the approximate designed values for Kvco, C_{int}, I_{nup} and I_{ndn} can be used in estimations. Using this assumption and further assuming that the change in voltage is approximately linear over a small range, the corresponding change in the loop filter voltage can be estimated as.

$$\Delta V_{ctrl} = \frac{\Delta f}{Kvco} \qquad \text{(V)}$$

Equation 3

Where: V_{ctrl} is the change in control voltage, and Kvco is the VCO gain parameter.

With the estimate for V_{ctrl} obtained, it can be converted to an expression in terms of expected time delay per comparison cycle as follows.

$$\Delta T_{cycle} \approx \frac{\Delta f \bullet C_{int}}{Kvco \bullet i \bullet N_{cycles}} \qquad \text{(s)}$$

Equation 4

Where: C_{int} is the expected capacitance, i is the charge pump current, and N_{cycles} is the number of cycles of the reference signal that Δf is measured over.

Equations 2, 3 and 4 follow a similar process to those provided in [1] for estimation of the static phase error due to finite bias currents.

Equation 4 was used to estimate the maximum time deviation of the PLL signal over 500 cycles of the 10 MHz reference waveform. Tabulated results for the total frequency and voltage deviations over 500 cycles and estimated time deviations over 1 cycle are given in table 5.

R_{leak}	ΔV_{CTRL}	Δf	ΔT_{CYCLE}
100 MΩ	6.26 mV	1.252 MHz	125 ps
10 MΩ	62.7 mV	12.5 MHz	1.25 ns
1 MΩ	490 mV	98 MHz	9.86 ns
1 MΩ over 250 cycles	313.5 mV	62.7 MHz	12.5 ns

Table 5 Estimates of maximum timing deviation.

Comparison of the in table 5 values with those given in table 3 shows a close correspondence for the 100 MΩohm and 10 MΩ case. The initial 1 MΩ case shows a marked deviation over 500 cycles. The deviation is due to non-linearity of the discharge slope over large values, that is, the control voltage saturated at its lower limit. If measurement of relative leakage was required in this situation the measurement time could be reduced. The same measurement over 250 cycles of the reference waveform is also provided. The results show that the method could be used to highlight faults that would lead to unacceptable performance degradation. It is the intention that suitable deviation limits would be decided upon in the PLL design phase. The methods were also carried out for CP mismatch of 20% (typical allowable deviation) in the down current source and 20% timing delays in the PFD input paths. In any case it is assumed that the matching will be quite good. For the CP mismatch case the performance was

still better than the 100 MΩ leakage resistance case. For the PFD delay mismatch the performance was still acceptable. It was initially concluded that as leakage in the forward path could be contributed by any of the elements, excessive errors in any particular component could be in the first order mapped to loop filter leakage.

4.4. Initial analysis of phase noise spur increase in terms of VCO modulation voltage:

The time values estimates in table 5 represent the effective time delay the closed loop CP-PLL will be trying to compensate for on each comparison cycle. Therefore in closed loop mode, and for a constant leakage or negative bias on the loop filter node we will have the following operations over 1 cycle.

1) On the rising edge of the reference signal the UP current source switches on and attempts to inject current of amplitude I_{NUP} into the loop filter node.
2) When the delayed feedback edge occurs due to the constant leakage on the main integration capacitor, at ΔT_{cycle} (see table 5) the UP current source switches off and both the up and down current sources are off. Thus the loop filter node is ideally isolated and the control voltage should remain at the voltage level on the main loop filter capacitor C_{int}.
3) Because of the leakage on C_{int}, the control voltage is reducing over the remaining part of the comparison cycle.

So for example if the closed loop PLL were operating in conditions with a 1 MΩ leakage resistance in parallel with C_{int} (see table 5 also) and a reference frequency (Fref) of 10 MHz we would have.

$$\Delta T_{cycle} \approx 12.5ns$$

and

$$\Delta T_{leak} \approx \frac{1}{Fref} - \Delta T_{cycle} \approx 87.5ns$$

Equation 5

Where:ΔT_{leak} is the effective time leakage can occur for.

To illustrate the PLL action in the presence of leakage simulation plots of the loop filter control voltage deviation, the reference the feedback and current source signals are shown in figure 9 over 3 periods of the reference waveform.

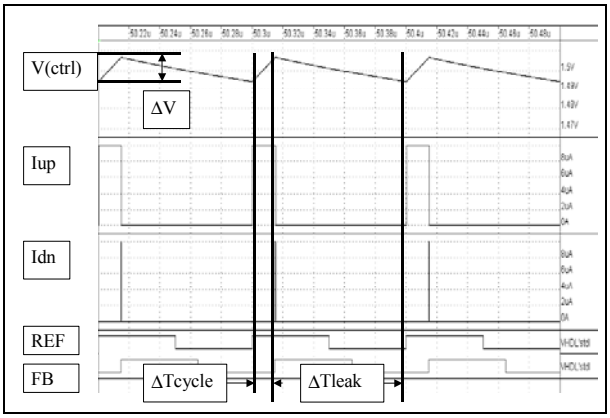

Figure 9 Illustration of loop filter leakage

In figure 9, ΔV indicates the approximate amplitude of the 10 MHz ripple voltage present on the loop filter node.

The ripple voltage on the loop filter node (the VCO control node) due to the leakage can be considered in the first instance as a modulating signal present on a VCO control input. That is, for first approximations the system output can be viewed in terms of a frequency-modulated spectrum of an open loop VCO with an appropriate modulation input. [2][4][43]. This assumption works well for initial sideband spur locations and amplitude approximations. However in a closed loop situation the PLL still tends to reduce the noise floor of the open loop VCO.

Thus, the initial problem after calculating the time offset was to estimate the modulating voltage on the VCO control line with the PLL operating in the closed loop mode.

The closed loop modulation was initially estimated using the values for ΔT_{cycle} from table 5 as a starting point. In addition, the following assumption is used.

When the PLL is in a closed loop mode the control voltage is maintained primarily on Cint with an average value to keep the VCO output at the desired average operating frequency. This is a valid assumption as long as the leakage effect is not excessive (see table 2).

Using this assumption the average value per cycle on C_{int} is given by.

$$V_{ave} = \frac{fout}{Kvco} \qquad (v)$$

Equation 6

Where: fout is the desired operating frequency, V_{ave} is the required voltage to maintain this frequency and Kvco is the VCO gain in MHz / V and is given in table 1

So the required operating frequency to maintain fout at 300MHz is 1.5V.

To continue with the approximate control voltage amplitude calculations the operation of the loop filter

node components for ΔT_{cycle} is considered in each individual reference cycle.

Referring to figures 1 and 9 the average voltage on the control line will be 1.5V before Iup turns on. Also, I_{Nup} will turn on for the time predicted from table 5. To find the ripple magnitude due to I_{Nup} the loop filter impedance is initially found in the Laplace domain and multiplied by the required input function.

$$V_o(s) = \frac{Iup(s)}{s} \cdot \frac{s \cdot Rd \cdot C\,\mathrm{int} + 1}{s^2 \cdot Rd \cdot C\,\mathrm{int} \cdot Cg + s \cdot Cg + s \cdot C\,\mathrm{int}}$$

Equation 7

Taking the inverse Laplace transform of equation 7 provides an initial estimation for the ripple amplitude of the VCO control voltage. The result is shown in equation 8.

$$v_o(t) = Iup\left(\left[\frac{1}{(Cg+C\mathrm{int})^2} \cdot Rd \cdot C\mathrm{int}^2 + \frac{1}{(Cg+C\mathrm{int})}t - \frac{1}{(Cg+C\mathrm{int})^2}\right] \times \quad Rd \cdot C\mathrm{int}^2 \cdot \exp\left[-(Cg+C\mathrm{int}) \cdot \frac{t}{Rd \cdot C\mathrm{int} \cdot Cg}\right]\right) \text{(V)}$$

Equation 8

The value calculated from equation 8 is added to the approximate control line voltage.

Table 6 shows approximate estimates of the ripple magnitude and the corresponding values for the various values of ΔT_{cycle}. The measurements were taken over ΔV (see figure 9).

Rleak	ΔTcycle	Measured ΔV	Estimated ΔV
1 MΩ	12.5 ns	12.3 mV	12 mV
10 MΩ	1.25 ns	1.3 mV	1.247 mV
100 MΩ	125 ps	140.5 uV	125 uV

Table 6 Loop filter ripple magnitudes.

In terms of frequency modulation the values of table 6 can be used to estimate the modulation factor and hence find the approximate spur amplitudes of the VCO output spectrum. This can be achieved as follows.

The VCO / PLL output signal fout can be described as.

$$v_c = V_c \sin[2\pi \cdot f_c \cdot t - mf \cos(2\pi \cdot fm \cdot t)]$$

Equation 9

Where: v_c represents the modulated output signal or fout in this case, Vc represents the amplitude of the modulated output signal, f_c is the nominal frequency of the carrier signal, fm is the frequency of the modulating signal and mf is the modulation factor.

Equation 9 represents a frequency modulated carrier signal. The modulation factor is described [43] as

$$mf = \frac{\Delta fc}{fm}$$

Equation 10

Where: Δfc is the total change in the carrier frequency and fm is the frequency of the modulating signal.

So in the case of the PLL with leakage the modulation factor is approximately.

$$mf = \frac{\Delta V \cdot Kvco}{Fref}$$

Equation 11

Where: ΔV is the approximated amplitude of the ripple voltage, Kvco is the VCO gain, and Fref is the frequency of the PLL reference signal.

For frequency-modulated signals where the modulation signal is a cosine wave (as in equation 9) the relative amplitudes of the spur signals in the output spectrum can be found using Bessel functions. Bessel functions are usually tabulated for various values of modulation factor [43].

The sidebands are spaced symmetrically at multiples of the modulating frequency from the carrier. From observation from tabulated results it can be shown that the relative amplitudes of the first two sidebands for a modulation factor up to 0.6 can be found using the approximations [4].

$$J_0(mf) \approx 1$$

$$J_1(mf) \approx \frac{mf}{2}$$

$$J_2(mf) \approx \frac{mf}{8}$$

Equation 11

Where: J_N represents the Bessel function value that is used to scale the carrier signal amplitude.

The Bessel function provides an initial approximation for a cosine wave-modulating signal. However, observation of figure 9 shows that the actual modulating signal is in the form of an approximate ramp function. In this case the frequency-modulated spectrum is more complex. Despite this difference the approximation of using a cosine wave for the modulating signal can provide good initial estimations of sideband spur amplitudes and where problems may occur.

The values from table 6 were used to initially calculate the modulation factor using equation 11. The results

were then used to approximate the expected sideband dB amplitudes. Values are provided in Table 7.

Rleak	ΔV (measured)	mf	Spur 1	Spur 2
1 MΩ	12.3 mV	246×10^{-3}	18dBc	42dBc
10 MΩ	1.3 mV	26×10^{-3}	37dBc	81dBc
100 MΩ	140.5 uV	2.81×10^{-3}	57dBc	120dBC

Table 7 Predicted spur values.

Figure 10 shows the respective frequency spectrums plots of the PLL output waveforms for the 1 MΩ and 100 MΩ leakage resistance values.

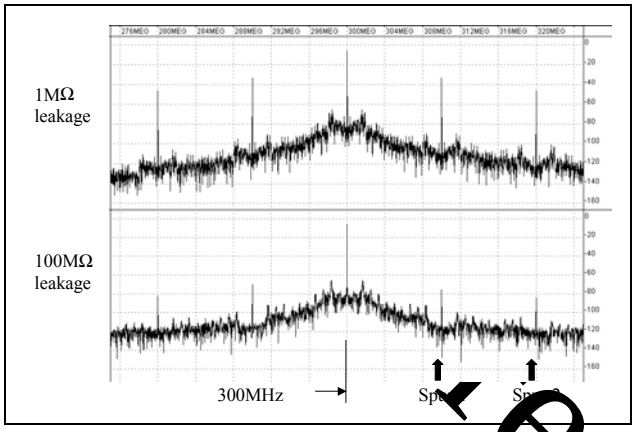

Figure 10 Frequency spectrum plots for 1 MΩ and 100 MΩ leakage resistances

The measured dB spur values taken with respect to the carrier are provided in table 8.

Rleak	Carrier	Spur1	Spur2
1 MΩ	-6.064 dB	27 dBc	40 dBc
10 MΩ	-6.046 dB	46 dBc	59 dBc
100 MΩ	-6.045 dB	69 dBc	78 dBc

Table 8 Relative spur values

The values in table 8 show a reduction in the spurs with increasing values of leakage resistance as would be expected. However, the values differ from the theoretically predicted values of table 7. Differences in values are primarily due to the approximation in the modulation signal used. A ramp type-modulating signal such as the one depicted in figure 9 will consist of more harmonic components, which will effectively spread the spectrum of the spurs and thus decrease the strength of the main spur signal. Additionally, the PLL's compensation action and loop filter will still (even though the PLL is in error) assist in suppressing the generated spurs.

The preferred method for using the suggested open loop leakage measurements techniques and associated ΔT_{cycle} estimates for spur prediction would be with the use of corresponding behavioural models to allow estimation of the maximum leakage that could be tolerated for a particular application.

Similar techniques to the ones explained can also be used for detection of unequal or excessive charge pump mismatch. Suitable sequences that would allow the estimation of ΔT_{cycle} due to charge pump mismatch are explained in [12]. In the leakage estimate technique shown here the measured value includes both leakage from the loop filter node and positive or negative biases due to the charge pump current mismatch. This can be understood by observing figure 8. Using this arrangement both charge pump current sources will switch on simultaneously for a finite time on the coincident edges of the input signals. In this situation if one of the current sources is stronger than the other current source the loop filter voltage will be biased in one direction in a similar manner to the loop filter leakage case. Several options exist to separate the leakage effects due to charge pump mismatch and loop filter leakage if this is desired. A typical method is outlined below.

- Deactivating both current sources simultaneously will allow measurement of leakage from the loop filter node when it is in the high impedance state. Opening the PLL loop and applying single coincident edges to the PFD inputs after lock has been achieved can perform this operation.

Subtracting the value of the frequency deviation using this method from the one depicted in figure 8 will provide an indication of the charge pump leakage.

This procedure is provided for example, however, in most situations the total deviation per cycle will be the most important factor. Further experiments were carried out relating to 5% and 10% and 20% charge pump mismatches. In these cases the close in phase noise spectrum around the carrier was degraded, however, the performance was still better than the leakage resistance cases.

5. Conclusions and further work.

The paper has presented an investigation of the jitter output spectrum of a CP-PLL when it is under the influence of faults that lead to deterministic jitter at the PLL output. There is obviously a strong correlation between loop filter leakage and performance degradation of the PLL. It is also likely that errors could occur in the loop filter elements when considering fully embedded CP-PLL implementations. In consequence it seems sensible to carry out leakage tests prior to more advanced tests.

The paper has discussed the possibility of detecting the typical faults using simple measurement techniques and relating them back to PLL signal output degradation. The estimates for the per cycle offset are accurate and have been extended to approximate the likely loop filter ripple. It is the intention that spur increase prediction is

to be investigated in more detail to ultimately yield more accurate predictions.
It is the intention that further work be carried out into investigation of a closed form solution of jitter related to output frequency deviation in the emulated open loop mode. In addition jitter measurement of the PLLs open loop oscillator and the relationship of the jitter to closed loop operation is to be carried out. The goal is to attempt to enable tests for full system performance to be carried out using simpler methods on a desensitised and decomposed PLL.
Other work is currently being undertaken towards evaluation of PLL output signal determination due to coupled noise effects and the development of techniques useful for highlighting these effects.

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