Electronic CAD Practical work

Dr. Martin John Burbidge
Lancashire UK
Tel: +44 (0)1524 825064
Email: martin@mjb-rfelectronics-synthesis.com

Week 1: Introduction to transistor models

curve tracing of NMOS transfer characteristics

Important course note:

All following lab session material is based upon lectures given in the Electronic Circuit Engineering lectures, and as such you are expected to bring copies of your lecture notes into the lab sessions. The primary intention of the course is to reinforce your understanding of lecture material through circuit simulation.

Objectives:

- To provide an introduction to the SPICE level 1 transistor model.
- Provide an introduction to the MOSFET symbols used in the simulator.
- To provide an overview of how to set up model parameters.
- Provide an insight into how changing the W/L ratios of a MOSFET transistor affect its operating characteristics. We will specifically look at the MOS DC transfer characteristic curves relating I_D (drain current) to V_{GS} (gate source voltage) and V_{DS} (drain source voltage).
- Introduce simple MOSFET parameters in the SPICE simulation environment, such as VTO (threshold voltage), KP (conductance parameter), W (channel width), L (channel length) and LAMBDA (channel length modulation parameter).

Aims:

At the end of this exercise the student should be able to.

- Recognize and change simple level 1 MOSFET parameters.
- Recognize what physical parameters may change the electrical characteristics of a particular MOSFET.
- Relate the above points to changes in the operational characteristics of the MOSFET.

Introduction To the MOSFET as Used in Simulations:

The MOS Transistor can be formed as one of two types:

- NMOS or
- PMOS

Each transistor will either be an enhancement mode or a depletion mode device.
In all the exercises that follow we will consider enhancement mode devices.

All MOS Transistors are 4-terminal devices. The four terminals of the transistor are listed below.

- DRAIN
- SOURCE
- GATE
- SUBSTRATE

Note that: The MOS transistor is often depicted as a 3 terminal device in schematic symbols, with the substrate connection being tied to the following terminals:

- Source (for an NMOS transistor)
- Source (for a PMOS transistor)

For many designs, the substrate connection will be connected to one of the power supply rails (V_{DD} for the PMOS and V_{SS} for the NMOS) to prevent any forward biased p-n junctions in the circuit.
The symbols and connection details for PMOS and NMOS transistors used in the simulation package are shown below.
Note: Other symbols are used but they will not be discussed here

Figure 1

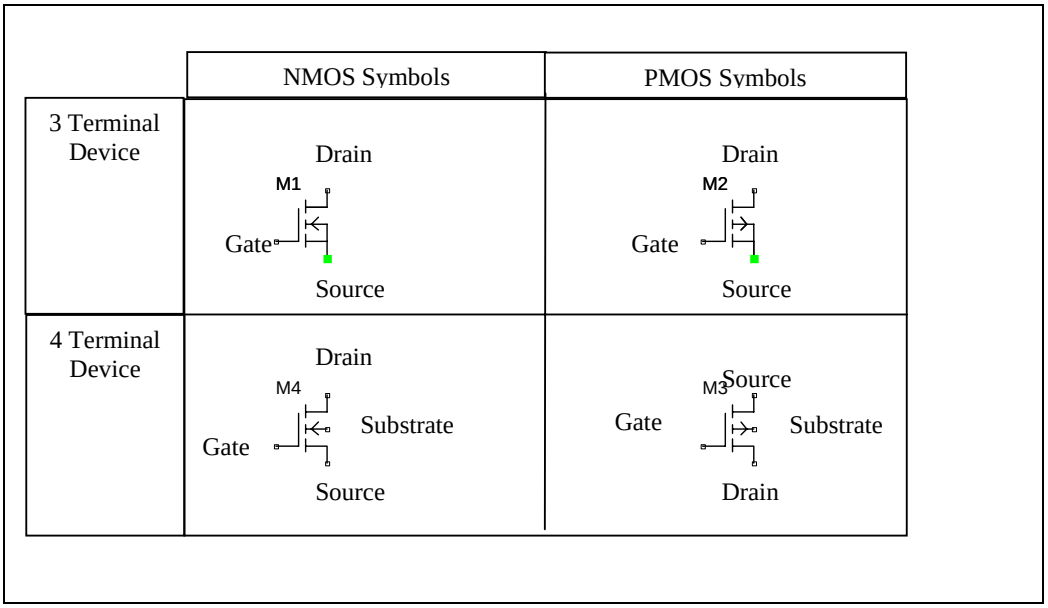


Figure 1: Depicting MOS symbols used in the simulation package.

In the above diagram the arrow indicates the p-n junction formed between the substrate material and the gate and source terminals of the transistor. You may recall the following transistor features from lectures:

- For a NMOS:
  - The source and drain terminals are constructed from n-type material.
  - The substrate is constructed from p-type material.
- For a PMOS:
  - The source and drain terminals are constructed from p-type material.
  - The substrate is constructed from n-type material.

Thus using an NMOS transistor as an example;

If the substrate was set at a higher potential voltage than the source or drain terminals, the p-n junction would be forward biased allowing conventional current to flow in the direction of the arrow. The opposite argument is true for the PMOS transistor.

Overview of the MOSFET Models used in SPICE

There are various MOSFET models used by SPICE style simulators. The most commonly encountered MOSFET models are outlined below.

- **Level 1:** The "Schichman-Hodges" model: This model is based upon the simple first order MOSFET formulae that you have been introduced to in lectures. It is a basic model that is suitable for preliminary circuit analysis. For example, this model may be used to carry out the "first pass" simulation run on a large integrated circuit design to ensure that the circuit is connected and functionally correct.
- **Level 2:** The "Analytical model" is a geometry-based model developed from one dimensional device physics and includes moderate two dimensional corrections. This model has limitations for smaller device geometries.
- **Level 3:** The "Semi-empirical model" is a more qualitative model that uses observed operation (i.e. measurements of real devices) to define its equations. This approach proved to be effective in including small geometry effects.
- **Level 4:** "BSIM" (Berkeley short channel IGFET model) advances the semi-empirical approach, with over 60 parameters used to describe electrical operation and the effects of geometry.

Other model levels exist for different simulation packages. However, the four levels outlined above are usually supported.
As the model level is increased the complexity of the model also increases. The BSIM model is the most advanced, and is subject to constant development. At present the BSIM4V1 model is the most current, this model is able to produce accurate simulation results for deep sub micron technologies. However, there is a trade off between accuracy and speed, and in general simulation times for non-trivial circuits take more time when using the more advanced models. In addition, problems may occur due to simulator convergence.

The semi-empirical models are used almost exclusively in industry to provide accurate results. The empirical data for the models is extracted by taking actual measurements from fabricated circuits. The data is then inserted into the transistor models, to produce a "design kit". In general, a circuit designer will be supplied with a "design kit" that relates to a particular process technology.

The Level 1 MODEL Parameters:

The table below illustrates the parameters related to the Level 1 MOSFET model. Note that these parameters also relate to the level 2, and 3 models. The BSIM models include other parameters, but these will not be discussed at yet.

Table 1

NAME	PARAMETER	UNITS	DEFAULT	EXAMPLE
LEVEL	model index		1	
VTO	**zero-bias threshold voltage**	**V**	**0.0**	**1.0**
KP	**transconductance parameter**	**A/V2**	**2e-5**	**3.1e-5**
GAMMA	bulk threshold parameter	V1/2	0.0	0.37
PHI	surface potential	V	0.6	0.65
LAMBDA	**channel-length modulation (level 1 & 2 only)**	**1/V**	**0.0**	**0.02**
RD	drain ohmic resistance	ohms	0.0	1.0
RS	source ohmic resistance	ohms	0.0	1.0
CBD	zero-bias B-D junction capacitance	F	0.0	20fF
CBS	zero-bias B-S junction capacitance	F	0.0	20fF
IS	bulk junction saturation current	A	1.0e-14	1.0e-15
PB	bulk junction potential	V	0.8	0.87
CGSO	gate-source overlap capacitance per meter channel width	F/m	0.0	4.0e-11
CGDO	gate-drain overlap capacitance per meter channel width	F/m	0.0	4.0e-11
CGBO	gate-bulk overlap capacitance per meter channel length	F/m	0.0	2e-10
RSH	drain & source diffusion sheet resistance	ohm/area	0.0	10.0
CJ	zero-bias bulk junction bottom capacitance per meter2 junction area	F/m2	0.0	2e-4
MJ	bulk junction bottom grading coefficient		0.5	0.5
CJSW	zero-bias bulk junction sidewall capacitance per meter junction perimeter	F/m	0.0	1.0e-9
MJSW	bulk junction sidewall grading coefficient		0.5, 0.33 (level1), (level2,3)	
JS	bulk junction saturation current per meter2 of junction area	A/m2		1.0e-8
TOX	**oxide thickness**	**meter**	**1.0e-7**	**1.0e-7**
NSUB	substrate doping	1/cm3	0.0	4.0e15
NSS	surface state density	1/cm2	0.0	1.0e10
NFS	fast surface state density	1/cm2	0.0	1.0e10
TPG	type gate material(+1 if opp. substrate, 0 if A1 gate, -1 if same as substrate)		1.0	
XJ	metallurgical junction depth	meter	0.0	1

LD	lateral diffusion	meter	0.0	0.8
UO	surface mobility	cm2/Vs	600	700
UCRIT	critical field for mobility degradation (level2 only)	V/cm	1.0e4	1.0e4
UEXP	critical field exponent in mobility degradation (level2 only)		0.0	0.1
UTRA	transverse field coefficient (deleted for level2)		0.0	0.3
VMAX	maximum drift velocity of carriers	m/s	0.0	5.0e4
NEFF	total channel-charge (fixed and mobile) coefficient (level2 only)		1.0	5.0
KF	flicker noise coefficient		0.0	1.0e-26
AF	flicker noise exponent		1.0	1.2
FC	coefficient for forward bias depletion capacitance formula		0.5	
DELTA	width effect on threshold voltage (level2,3)		0.0	1.0
THETA	mobility modulation (level3 only)	1/V	0.0	0.1
ETA	static feedback (level3 only)		0.0	1.0
KAPPA	saturation field factor (level3 only)		0.2	0.5
TNOM	parameter measurement temperature	deg. C	27	50

Table 1 *Illustrating SPICE Transistor model parameters.*

Note: The above parameters are generally shared between transistors fabricated within the same integrated circuit, and as such the designer has no control over them. **The designer can alter other parameters specific to an individual transistor, such as the width and length.**

Equations and Parameters relating to the Exercises:

For many of the exercises we will only be using a few of the parameters from table 1. In addition we will be modifying the width and length of the transistor channel. The parameters of interest along with the associated equations are given below.
Parameters for exercises:

Spice Parameter	Description	Units
VTO	Zero-bias threshold voltage	Volts
KP	Transconductance Parameter	A/V^2
LAMBDA	Channel Length Modulation	V^{-1}
W	Channel width	M
L	Channel Length	M

Notes: Further parameters will be investigated as the course progresses.
KP in SPICE is equal to $u_{(n \text{ or } p)}$ multiplied by C_{ox}
If VTO is not given it is calculated from other process dependant device parameters.

First order MOSFET equations:

The MOSFET operates in the following regions:

- **Linear region** (or triode region)
- **Saturation region**

The particular region that the transistor will operate in is related to the drain source voltage (V_{DS}) and the threshold voltage (VTO).
Note: That VTO in this document is equivalent to V_{THN} or V_{THP} in the lecture notes.
The equations that relate the drain current of the transistor to the gate voltage are given below. Note: that the initial equations relate to an NMOS device.

Linear Region:

$$I_D = KP \cdot \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right] \qquad \text{for } V_{GS} \geq V_{TH} \text{ and } V_{DS} \leq V_{GS} - V_{TH}$$

Saturation Region:

$$I_D = \frac{KP}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH})^2 \qquad \text{for } V_{GS} \geq V_{TH} \text{ and } V_{DS} \geq V_{GS} - V_{TH}$$

Where KP is the transistor transconductance parameter and is defined by the equation below:
For an **N-channel MOSFET:**

$$KP_n = \mu_n \cdot C'_{ox} = \mu_n \cdot \frac{\varepsilon_{ox}}{TOX}$$

and for a **P-channel MOSFET:**

$$KP_p = \mu_p \cdot C'_{ox} = \mu_p \cdot \frac{\varepsilon_{ox}}{TOX}$$

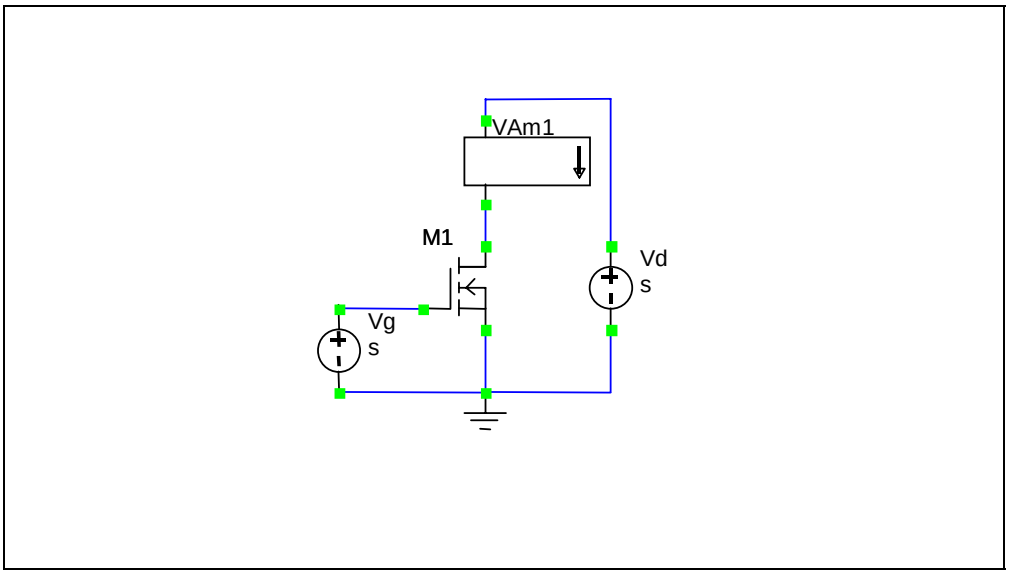
Where:
μ_n, is the mobility of the electrons in an NMOS transistor.
μ_p, is the mobility of the holes in a PMOS transistor.
C'_{ox}, is the capacitance of the gate oxide. i.e. the capacitance formed between the gate and the channel.
ε_{ox}, is the permitivity of the gate oxide.
TOX is the thickness of the gate oxide.

Note: The mobility of electrons is greater than the mobility of holes. Therefore, for the same size transistors, an N-channel device will carry more current. This can be seen by inspection of the equations above.

Exercise 1: Transfer Curves for an NMOS transistor: I_D versus V_{DS} for different values of V_{GS}

In this exercise you are going to plot the transfer characteristics of a MOSFET transistor.
For the circuit below the transistors can be found as follows:
Toolbar >> More Devices >> MOSFET(LEVEL 1 nmos)

Figure 2



Draw the schematic of figure 2.

Then set up the transistor properties as follows (only enter the boldface values)

Instance Properties:
L = 1u (m)
W = 2u (m)

Shared Properties:
VTO = 0.7 (v)
KP = 34e-6 (A/V^2)

Leave all the other values alone.
Note: Later we will change LAMDA. In this experiment LAMBDA defaults to zero.
Now try to set up a simulation using the dual parameter sweep in the set up simulations dialogue box.
The simulation should perform the following:

Set V_{GS} to step from 0 to 5 volts in 0.5 volt increments.

Sweep V_{DS} from 0 to 10 volts in 0.1 volt increments for each of the above values of V_{GS}.

When you have completed the above, run the simulation.

You should see a graph similar to the one in figure 3 below.
Figure 3:

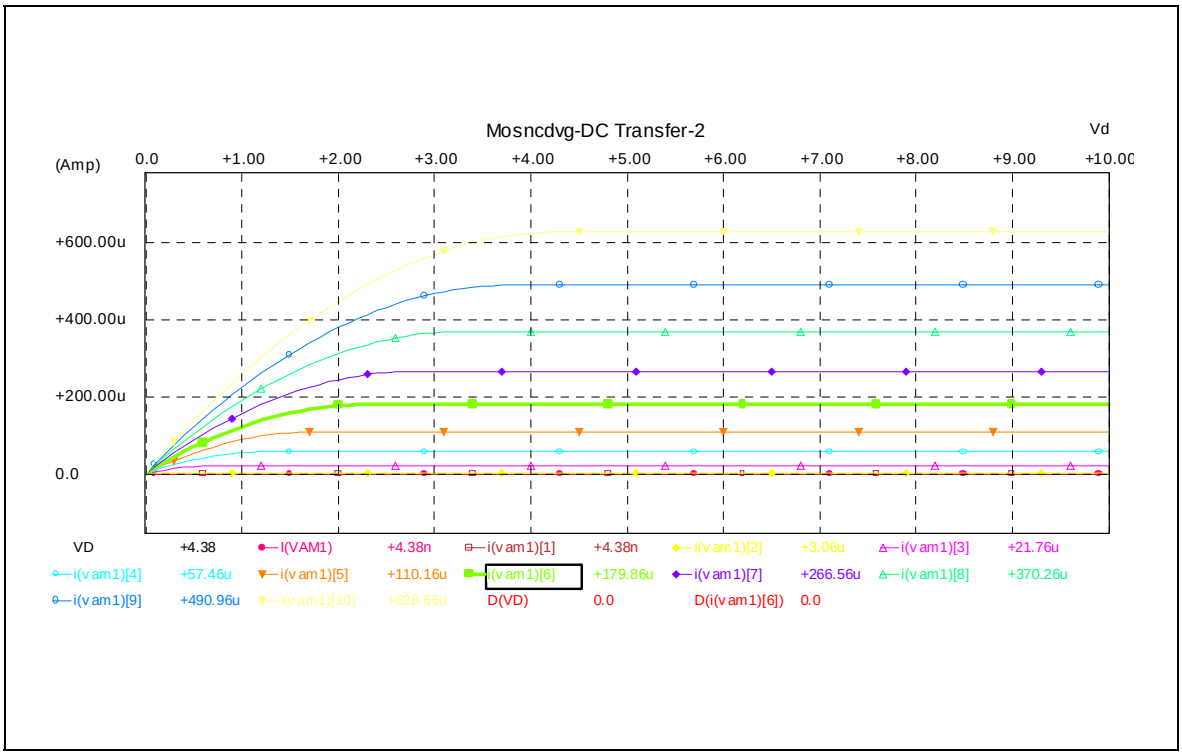


Figure 3: *Showing I_D versus V_{DS} curves for differing values of V_{GS} .*

Note: in the above graph each of the curves represents a different value of V_{GS}.

Question 1

A. Describe the operation of the transistor at the varying values of V_{GS} and V_{DS} in terms of the voltages and currents observed.
B. For each value of V_{GS} in the graph; try to ascertain the point at which the transistor moves from the linear to saturation region. Hint: this can be done from the equations.
C. Assuming that you can only change the width of the transistor:
Alter the transistor so that it has a drain current of 1mA whilst in saturation for a corresponding V_{GS} value of 2.5 volts. Verify your calculations by re running the simulation. What minimum value must V_{DS} be at to ensure that the transistor remains in saturation.

Exercise 2: Effects of channel length modulation:

When using the first order formulae on page 6 to model the MOSFET, the drain current remains constant for values of V_{DS} above V_{DS}(sat).
Note: $V_{DS}(sat) = V_{GS} - V_{TH}$

In reality, the drain current of the MOSFET in saturation does increase slightly as V_{DS} is increased. This effect occurs because the effective channel length decreases for

increasing V_{DS} and a shorter channel will possess a smaller resistance and thus allows a larger current to flow. This is one of the many second order effects that can be modeled using the level 1 SPICE MOSFET model.
In the SPICE level 1 MOSFET model the parameter that models this effect is called LAMBDA (channel length modulation parameter).
The modified equation for the MOSFET drain current including LAMBDA is given below:

$$I_D = \frac{KP}{2} \cdot \frac{W}{L}[(V_{GS} - V_{TH})^2 \cdot (1 + LAMBDA \cdot V_{DS})]$$

Question 2:

Note: before carrying out this exercise, ensure that the length and width of the NMOS transistor are set to 1u and 2u respectively.

A. In the transistor model, set LAMBDA = 0.02. Re-run the simulation of exercise 1. Highlight any differences from the simulations in exercise 1.

Answers Week1 Lent term

Question 1

A.

B.

C.

Question 2

A.