Section1.
Basic Measurements.

Author Details:

Dr. Martin John Burbidge

Lancashire
United Kingdom

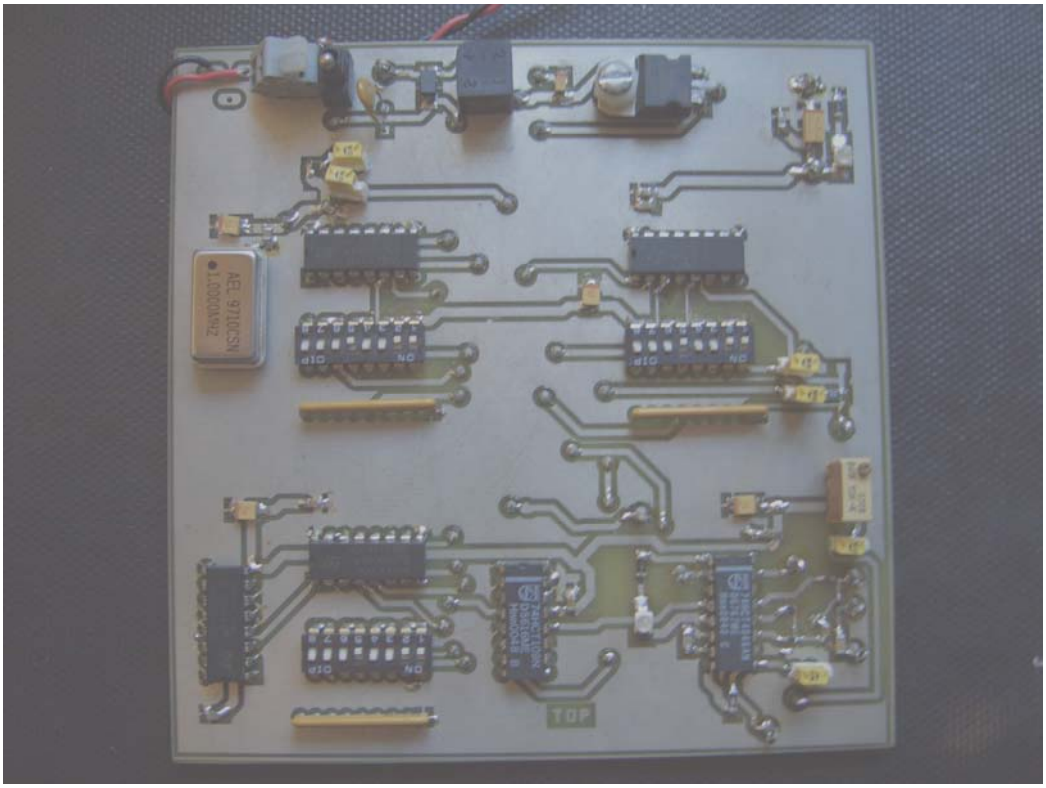
Tel: +44 (0)1524 825064

Email: martin.@mjb-rfelectronics-synthesis.com

Document Priority: Normal:
Associated Documents: Appendix 1; Pll demoboard Schematic.
Test Equipment: 0-30V Lab PSU; Oscilliscope-Agilent 54622D

Purpose:

The primary purpose of this lab session is to allow the student to assess the basic functionality of the PLL test demonstrator board. In addition, it will provide the student with familiarity of the test board and equipment setup prior to carrying out more advanced tests.



Contents

Section Contents

Figures and Tables

1.0 Introduction:

Aims:

The primary aim of this section of the practical module is to familiarise the student with the PLL test demonstrator board and the associated test equipment. In addition, this section will ensure that the hardware functions correctly before more advanced parts of the course are carried out.

Objectives:

After completing this practical module the student should be able to…

Using the Oscilloscope.

- ✓ Measure and verify correct operation of the various DC supply voltages to various part of the PLL test circuit.
- ✓ Measure and verify the main 5V supply voltage to the board.
- ✓ Measure the various output signals at various parts of the circuit, and verify correct amplitude and frequency of the signals.
- ✓ Investigate various divider settings of the circuit and verify that the frequency divider circuits operate correctly.
- ✓ Verify the static PLL operation for various loop divider settings.

Module Overview:

The primary purpose of this module is to assess correct functional operation of the PLL demonstrator board prior to its usage in subsequent practical modules. A secondary purpose of this module is to familiarise the student with the basic hardware and associated test equipment set-up.

Initially, this module will provide a diagram with a numbered indication of specific jumper, test point connections, and device pins, that are relevant to the particular tests. Then a description of the initial settings will be given.

The module will then be divided into separate sections covering the following test aspects.

Basic board tests:

1. Power supply voltages: External supply, and on-board supply.
2. Power to each component or board sub-block.
3. Master oscillator operation and frequency.
4. Reference divider for the master oscillator at different division settings.
5. Toggle divider, input and output frequencies.

PLL basic functional tests:

6. Output frequency for different feedback divider settings.
7. Loop filter voltage corresponding to the above settings.
8. Toggle operation relating to the PLL operation.

2.0 Basic Board Set-up:

This section outlines the initial jumper and divider settings that have to be made before commencing the test.

Warning: Before commencing any of the tests ensure that:

- The information supplied in Appendix 1 has been read, and understood.

The diagram below shows the topside silk screen of the PLL test demonstrator board, the outlined numbered sections indicate areas of the circuit that are of importance in this practical session.

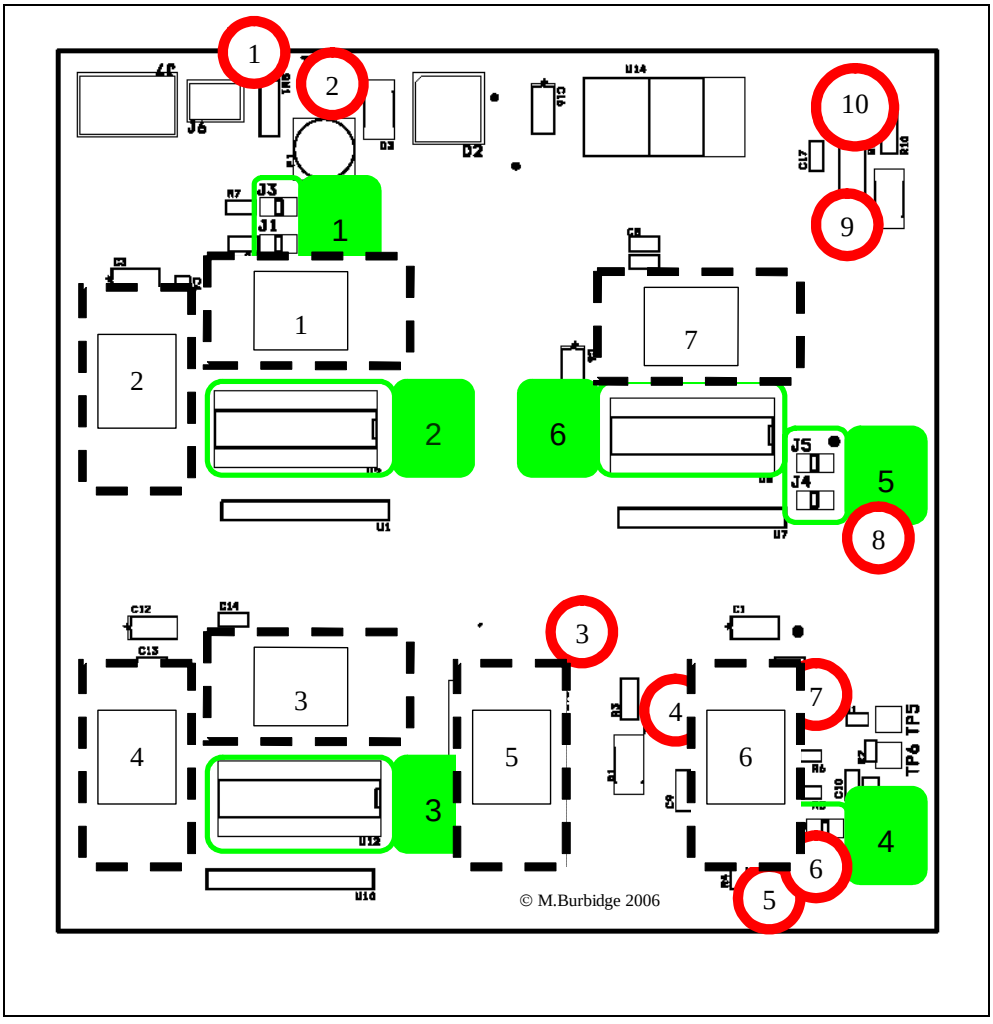


Figure 1Pll demonstrator board topside silkscreen with component details.

Note that in figure 1, the test pins are indicated by circles, the jumpers and switches are indicated by rounded rectangles, and components (**IC#**) are indicated by dashed rectangles. To aid identification, the components are numbered in an anti-clockwise direction.

With reference to figure 1 the table below explains initial jumper settings and switch details for this particular set of tests.

Jumper Block#	Associated components (Location)	Position details	Comments
1	J3 (Top) J1 (Bottom)	OFF ON	Isolates external reference.
2	U2 8way DIL Switch.	11101100 [1][2]	Divides the master oscillator by 20.
3	U12 8way DIL Switch.	11101100 [1][2]	Divides master oscillator by 200 then by 20.
4	J2	ON	Connects PLL loop filter node to VCO input
5	J4 (Bottom) J5 (Top)	OFF ON	Isolates the on board toggle signal from the PLL feedback divider
6	U8 8way DIL Switch.	11101100 [1][2]	Sets the PLL feedback divider ratio to 20.

Table 1 Initial jumper and switch connection details.

Notes:
[1] 1 = Switch in the on position.
0 = Switch in the off position.
[2] This is set to give an initial overall PLL feedback divider ratio of 40 (remember that the VCO output signal passes through a high speed divide by two element before being fed into the lower speed adjustable feedback divider).

Further information concerning connection details for a specific test will be covered in the following sections.

Test Hardware Physical set-up:

For this particular set of tests the test board should be powered from an external lab power supply that is set to supply a DC voltage in the range of 7-20 volts.
The oscilloscope for this set of tests will be used to probe various parts of the circuit.
Oscilloscope probe ground connections should be made to the test pin marked 9 in figure1.

An image of the Oscilloscope controls that will be used for reference in later parts of this module is given below.

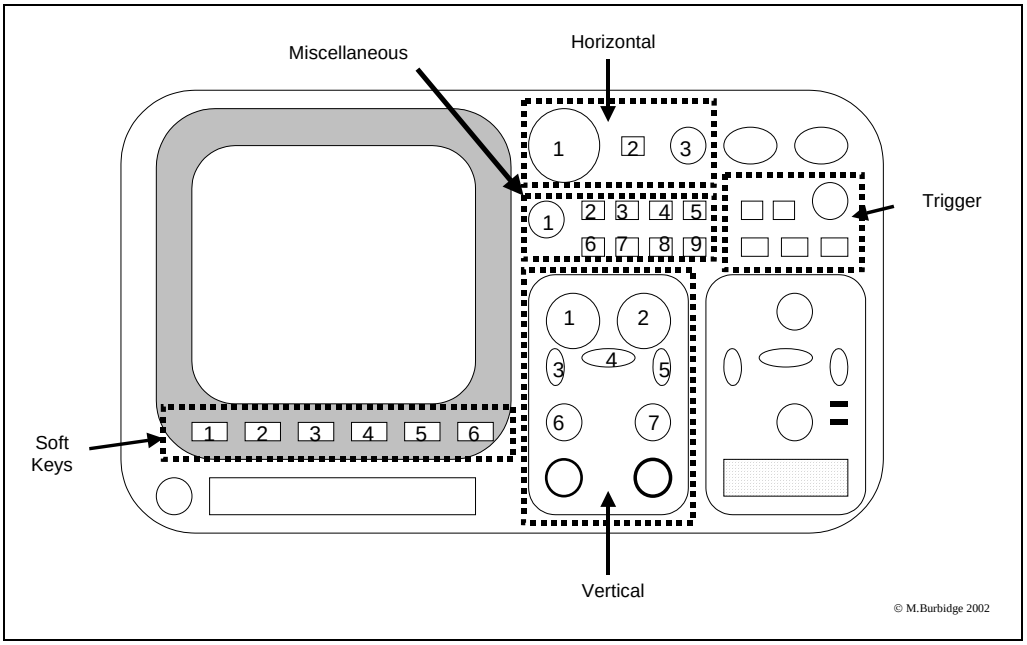


Figure 2Oscilloscope front controls

After the initial settings have been made and checked, the board can be powered up.
Note both LEDs (light emitting diodes) on the board should light up.
Now the experiments in the next sections can be carried out.
Reference to figures 1 and 2 is required for all of the following exercises.

3.0 Initial measurements:

Before carrying out further tests upon the PLL demonstrator board we need to ensure that all of the power supply voltages on the board are at the correct level. In addition, we need to check that all of the active components on the board are receiving the correct local supply voltage.

Main Power supplies:

For these measurements we are going to initially check the external power supply voltage that is supplied from the bench power supply. Then the locally generated 5-volt power supply will be measured.

External power supply:

Ensure that an oscilloscope probe is connected to the channel 1 connection of the oscilloscope and that the demonstrator board is powered up.

Oscilloscope settings:

Connect the probe tip to Test point 2 in figure 1.
The initial oscilloscope settings can be loaded from the file "QFILE_00" on floppy disk using the following buttons on the oscilloscope.
Save/Recall =>Recall =>From QFILE_00

You should now see a horizontal trace on the scope and the average DC voltage value of the signal should be displayed.

Ensure that the value of this signal is approximately 10 volts.

On board power supply:

Oscilloscope settings:

Connect the probe tip to Test point 10 in figure 1.
With reference to figure 2.
Change the vertical resolution to 1 volt per division by adjusting…

Vertical=>1=> Adjust the knob clockwise until the number in the top left hand corner of the screen changes to 1.00V.

Ensure that the value of this signal is between 4.95 and 5.05V.

Individual active component power supplies:

Keeping the same oscilloscope settings of the previous section, remove the oscilloscope probe tip cover, and check the voltage on each of the active components power supply pins.

Note: That the device pins are numbered from the index mark (pin1) in an anticlockwise direction.

With reference to figure 1, details of the specific power supply pins are tabulated below.

Figure 1 location	Pin#
1	16
2	4
3	16
4	16
5	16
6	16
7	16

Table 2 Active component pin locations.

Before proceeding ensure that all of the supply pins have a voltage level between 4.9 and 5.1V.

4.0 Divider settings measurements:

In this section the basic functional operation of the various on board reference and frequency divider circuits will be measured.

Oscilloscope settings:

The initial oscilloscope settings can be loaded from the file "QFILE_01" on floppy disk using the following buttons on the oscilloscope.

Save/Recall =>Recall =>From QFILE_01

Further measurements should only require the changing of the horizontal resolution.

4.1 Master oscillator and reference divider settings:

Place the oscilloscope probe on Pin 1 of component 2.

You should see the following scope display.

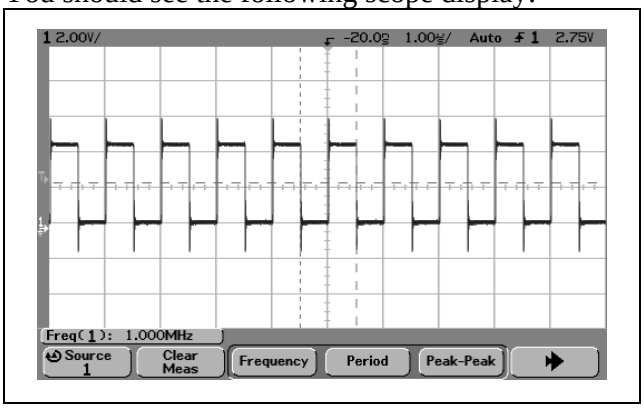


Figure 3Master oscillator signal.

Verify that the following measurements are correct.

Parameter	Value
Frequency	1.00MHz
Period	1us
Duty cycle	50%

Table 3 Measurement values for the master oscillator.

Now place the oscilloscope probe on pin 14 of component 2.
Adjust the time base control.
Horizontal => 1
Until the scope display is similar to that of figure 4.

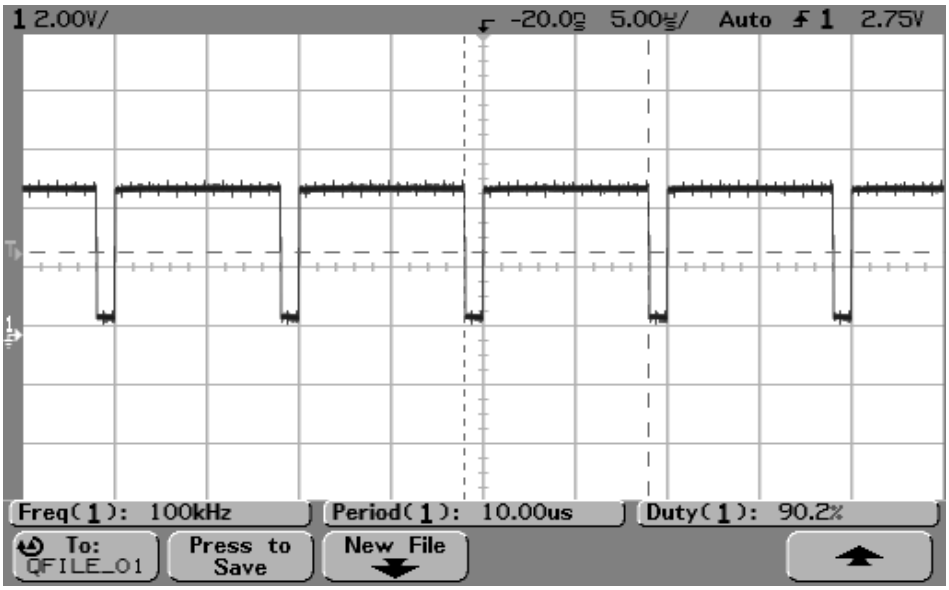


Figure 4Divided reference signal.

Parameter	Value
Frequency	50KHz
Period	20us
Duty cycle	90%

Table 4 Measurement values for the divided reference signal.

Note that this signal is used to provide the reference frequency signal for the phase locked loop circuit. Also, as the particular Pll circuit only operates on rising edges of the input signals, the duty cycle is unimportant.

Checking the reference divider switches:
Set up the reference divider circuit so that the divided down reference frequency is:
20KHz
10KHz
5KHz
Verify that the chosen switch settings produce the required frequencies.
Return the switches back to their original settings before proceeding.

4.2 Toggle divider measurements and settings.

The toggle divider circuitry consists of the following elements:

1. A **fixed divider** circuit (figure 1; IC4) that divides the frequency of the master oscillator signal by 200.
2. A **preset divider** (figure 1; IC3) that can be adjusted to divide the above signal frequency in a range from 2 to 257.
3. A **JK flip-flop** that converts the pulse from the above into a square wave signal.

The purpose of the toggle divider circuitry is to change the LSB (least significant bit) of the PLL feedback divider between 1 and 0, at a frequency determined by the combined division ratio of items 1, 2, and 3 above.

The purpose of this section is to evaluate the operation of the various divider circuits.

Oscilloscope settings:

Ensure that the channel 1 scope probe is connected and that the earth clip is connected to test pin 9.

The initial oscilloscope settings can be loaded from the file "QFILE_01" on floppy disk using the following buttons on the oscilloscope.

Save/Recall =>Recall =>From QFILE_01

Further measurements should only require the changing of the horizontal resolution.

Following table 5, the following measurements should be made on the components.

Description	Fig1 Location	Frequency	Period	Duty Cycle
Fixed divider input	IC4, pin1	1MHz	1us	50%
Fixed divider output / Presetable divider input	IC3, pin 1	5KHz	200us	99%
Presetable divider output / JK flip flop input	IC5, pin 4	250Hz	4ms	95%
JK Flip flop output	IC5, pin 7	125Hz	8ms	50%

Table 5 Measurement details for the toggle divider section.

Ensure that these measurements are correct before proceeding.

Checking the toggle divider settings:

Change the settings of the toggle divider switch to:

10, 100, 200

Then ensure that the output of the JK flip-flop alters to the expected value.

Questions:

1. What switch settings would produce a JK flip-flop output that is high for 2ms during each cycle of the waveform.

Return the switches back to their original settings before proceeding.

5.0 Basic functional PLL tests.

This section will concentrate upon making basic functional PLL measurements. The basic measurements will concentrate on verifying the PLL output frequency for various feedback divider settings. Recall, from the online notes and supporting material that the PLL output frequency should be an integer multiple of the reference frequency. Note that the feedback divider produces the multiplying factor.
In addition, to the basic functional tests, a functional test of the toggle divider action upon the PLL output response will also be made. However, the analysis of the response will be left until later modules.

Oscilloscope settings:
Ensure that the channel 1 scope probe is connected and that the earth clip is connected to test pin 9.
The initial oscilloscope settings can be loaded from the file "QFILE_01" on floppy disk using the following buttons on the oscilloscope.
Save/Recall =>Recall =>From QFILE_01
Further measurements should only require the changing of the horizontal resolution.

5.1 Feedback divider settings.

The initial settings for the divider network are as follows:

Component Description.	Fig1 location	Settings	Effective division ratio.
JK flip flop (set in toggle mode) from PLL VCO output to feedback divider input.	Pin 12, IC5, (JK input from PLL VCO output) Pin 9, IC5, (JK /Q output to feedback divider CLCK input)	Not applicable.	Divides by 2.
Feedback divider from JK flip-flop output to PLLFB input		b11101100 [1][2]	Divides by 20.

Table 6 Settings for initial PLL feedback divider tests.

Notes:
[1] 1 = Switch in the on position.
0 = Switch in the off position.
[2] This is set to give an initial overall PLL feedback divider ratio of 40 (remember that the VCO output signal passes through a high speed divide by two element before being fed into the lower speed adjustable feedback divider.

Following table 6, the following measurements should be made on the components.

Description	Fig1 Location	Frequency	Period	Duty Cycle
PLL output (JK input)	IC6, pin4	2MHz	0.5us	50%
JK output (main feedback divider input).	IC5, Pin9	1MHz	1us	50%
PLLREF input (feedback divider output)	IC6, Pin3	50KHz	20us	90%

Table 7 Basic measurement details for the PLL circuit.

Ensure that the following measurements are correct before proceeding.

Divider setting note:
In this set of measurements and experiments, the following parameters are set for the PLL feedback and reference divider system.

Parameter	Value
PLL Reference frequency	50KHz
Overall Feedback divider ratio	Adjustable between 40 and 60 in even values only [1][2][3].

Table 8 Reference and feedback divider settings.

Notes:
[1] So as to meet the PLL system operational requirements the divider should only be altered within this range.
[2] There is a fixed divider, so the actual switch settings are altered between 20 and 30.
[3] The output can only be even due to the presence of the JK flip flop (or divide by 2 element).

With reference to table 8 and recalling the relationship that:

Fout = N*PLLREF.

Where: fout is the PLL output frequency, N is the overall division ratio, and PLLREF is the reference.

It is possible to deduce that the PLL output can be made to produce 10, 100KHz spaced output signals that are between 2 and 3MHz.

Checking the feedback divider settings:
To range check, set the adjustable feedback divider ratio to 30 and verify that the output frequency of the PLL is correct.
Questions:

2. Change the feedback settings so that the PLL produces an output frequency of 2.5MHz. What switch value was used?

Keep the switch setting for the following experiment.

5.2 PLL Toggle divider setting check.

The purpose of the test explained in this section is to provide a simple functional indication of the toggle circuitry operation. The information from this section is simply used to verify that the toggle circuitry is connected correctly to the PLL feedback divider, and that it can be used to supply a frequency step input to the PLL circuitry. Analysis of the PLL step response will be left to later sections.

Before starting this test turn of the board and make the following adjustments to the jumper and switch settings.

Jumper Block#	Associated components (Location)	Position details	Comments
5	J4 (Bottom) J5 (Top)	ON OFF	Connects the on board toggle signal to the PLL feedback divider LSB.
6	U8 8way DIL Switch.	11100111	Sets the adjustable PLL feedback divider ratio to 25.

Table 9 Settings for basic functional PLL toggle test.

The settings of table 9 allow the PLL reference divider to be toggled between N and N+1 at a rate determined by the toggle divider settings. This action is effectively equivalent to applying a 100KHz frequency step at the PLL reference input.

Details of the test are as follows

Oscilloscope settings:

Ensure that the channel 1 scope probe is connected and that the earth clip is connected to test pin 9.

Ensure that the channel 2 scope probe is connected and the earth clip is connected to test pin 9.

The initial oscilloscope settings can be loaded from the file “QFILE_02” on floppy disk using the following buttons on the oscilloscope.

Save/Recall =>Recall =>From QFILE_02

Scope probe signal connections should now be made to the following points.

Description	Scope Probe	Fig1 Location
Buffered PLL loop filter node.	1	IC6, pin10
Toggle Signal.	2	Test pin 8

Table 10 Scope probe connections for functional PLL step test.

After the above connections have been made the board can be powered up.
If everything is working correctly, the oscilloscope should display the following image.

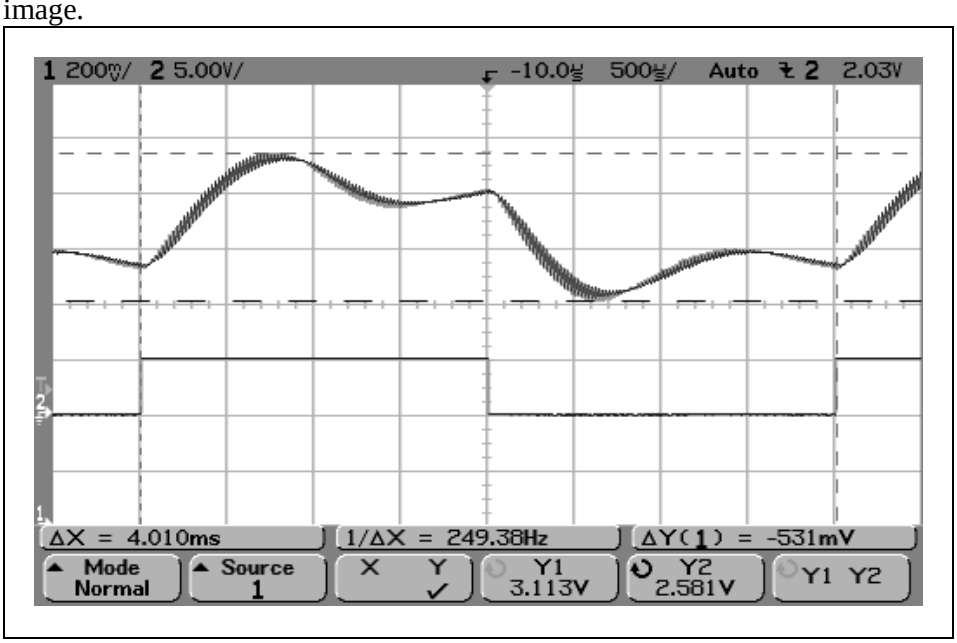


Figure 5Pll step response display.

After this image is displayed verify that the peak-to-peak output voltage of the channel 1 trace is approximately between 450 and 550mV.
Note: That due to device-to-device variations the actual value of the peak-to-peak voltage may vary significantly.

Basic Test Answer Sheet 1:

Student Name:……

Date:……..

This sheet relates to any in text questions that were asked in this practical.
If response plots or post processing graphs were requested, please name them and attach them to this sheet.

Answer#	
1	
2	
3	
4	
5	
6	
7	
8	
9	

Technicians set-up notes:

Equipment set up for this module consists of the following:

1) PLL demonstrator board connected to a bench power supply with an output of approximately 10V
2) Agilent 54622D oscilloscope with two scope probes.
3) Floppy disks containing scope set-up files.
    a. QFILE-00
    b. QFILE-01
    c. QFILE-02

    These files are contained in the local folder “InstumentFiles”.
    Further information for these files is contained in the text.