Section4:
PLL Transient Frequency Step Response.

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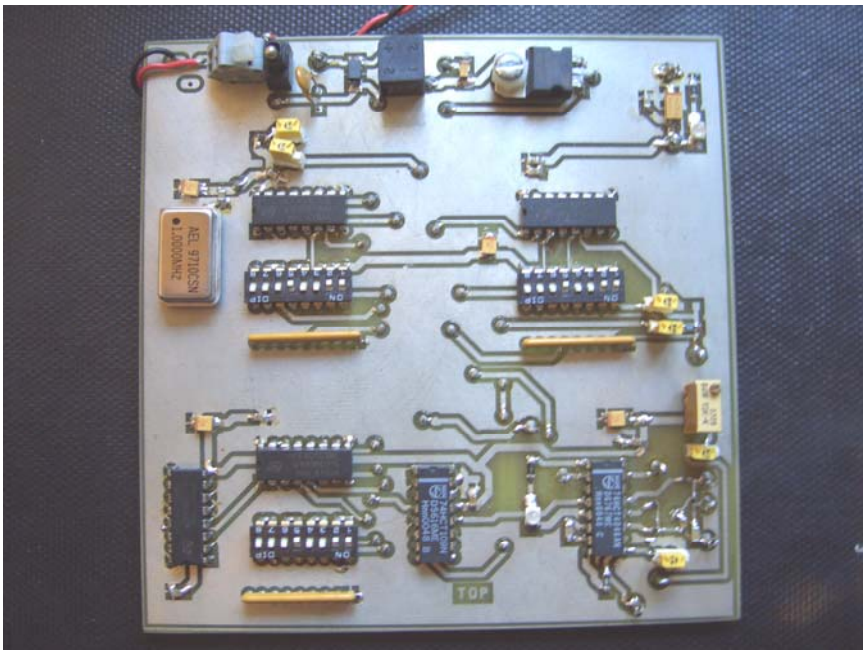
Document Priority: Normal:
Associated Documents: Appendix 1, PLLSimEqns.pdf ; Pll demoboard Schematic, Calculated VCO gains and measurements from lab session 2.
Test Equipment: 0-30V Lab PSU; Oscilloscope - Agilent 54622D + analogue probes and digital probes, RS232 lead and software.
Note: this document is for review purposes only. Some items have been deliberately removed

Purpose:
This module allows the student to investigate the PLL frequency step response.



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Figures and Tables

Introduction:

Aims:

The primary aim of this section of the practical module is to ……
Allow the student to carry out PLL frequency step response measurements and provide insight into some of the associated parameters.

Objectives:

After completing this practical module the student should be able to.

- ✓ Carry out PLL step response tests.
- ✓ Make simple measurements of over shoot, undershoot and settling time.
- ✓ Use simple equations to estimate damping and natural frequency of the PLL for different divider settings.

Prior work required:

Measurement of VCO gain, from module 2, estimation of ω_n and damping from PLLSimEqns.pdf, and some familiarity with the step response plots in the same document.

Module Overview:

In many of the mentioned applications the transient response of the PLL system when it is subjected to a frequency change on its input is of paramount importance. Thus, designers often use the frequency step response of the PLL as a primary characterisation tool. Monitoring of the PLL frequency step response can reveal important information relating to damping, natural frequency, overshoot, frequency settling time and phase settling time. Brief examples of the effects the mentioned parameters can have on system performance are provided below:

- The damping factor and the natural frequency will relate to how fast the PLL will settle to a steady output frequency or phase after it is subjected to a input frequency step change. An estimate of settling time can be found from these parameters.
- Frequency and phase settling times are usually measured between the time of application of the input step until the output step reaches a certain predefined value.

For high performance PLL's, overshoot is also often mentioned as a critical design parameter. Overshoot implies how high the PLL output frequency rises over its final steady state value after it has been subjected to a step input.
Generally PLL designers use appropriate equations and ideal response plots (see step response plots and equations for ωn and ζ in PLLSimEqns.pdf) in the initial PLL design phases to design a system to have a specific transient response. Then in the

characterisation phase, step response measurements will be carried out on the actual design, to ensure that the initial design constraints are met.

Figure 1 is used to illustrate the parameters of interest of a generic step response of a system.

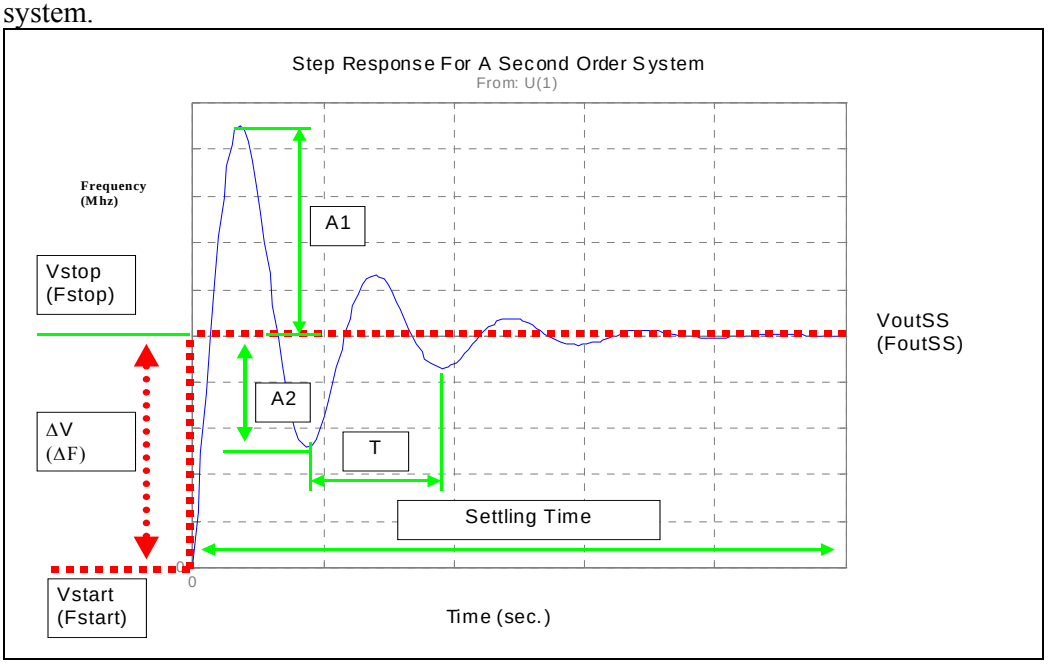

Figure 1 Generic transient step response.

Parameters in figure 1 are mentioned in terms of both voltage and frequency. However, remember that for PLLs we will be monitoring the output response due to a frequency step input. The critical parameters of figure 1 are outlined below.

- Vstart (Fstart): Is the voltage or frequency before the input step is applied.
- Vstop(Fstop): Is the final value of the input stimulus signal.
- ΔV(ΔF): Is the amount by which the input signal is changed.
- VoutSS(FoutSS): Represents the final steady state output value of the system.
- Settling time: The amount of time it takes after the application of the input step, for the system to reach its steady state value.
- A1: Peak overshoot of the signal.
- A2: Peak undershoot of signal.
- T: Time difference between the consecutive peaks of the transient response.

Direct measurement of these parameters can be used to extract ω_n and ζ. Estimation of the parameters is carried out using the following formulas that are taken from {1}. The formulas are valid only for underdamped systems ($\zeta < 1$) i.e. one in which A1,A2 and hence T can be discerned. However, if this case is not valid other parameters can be used to assess the system performance such as delay time, rise time and settling time. Additionally, in many applications what is really desired is the overall knowledge of the transient shape or signature of the system under test. The transient shape taken from oscilloscope plots can be compared against the graphs provided in PLLSimEqns.pdf.

Equation 1 **Estimation of damping factor from step response measurements. Taken from {1}.**

Equation 2 **Estimation of natural frequency from step response measurements. Taken from {1}.**

Note a Matlab file that calculates equations 1 and 2 above is included in the MATLAB directory related to PLLSimEqns.pdf .

A typical hardware set-up for step response monitoring of PLLs is illustrated below.

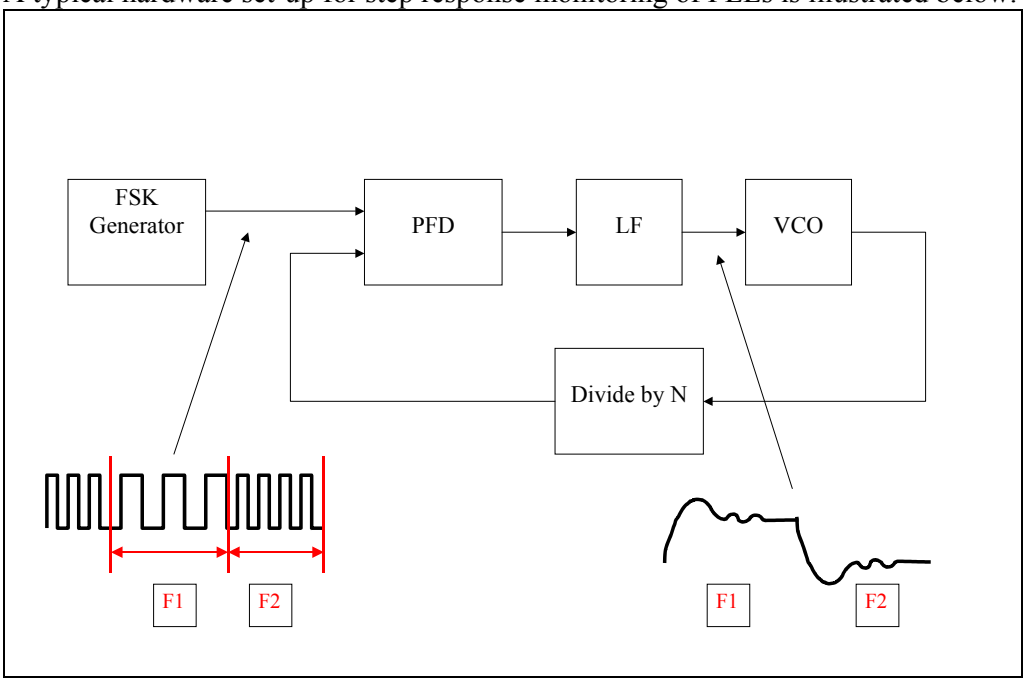

Figure 2Conventional PLL frequency step response bench set-up.

Further details relating to figure 2 are as follows:

The input signal step is applied by using a signal generator set-up capable of producing an FSK signal. The signal is toggled periodically between F1 and F2. Note that a suitable toggling frequency will allow the system to reach the steady state condition after each step transition.

For the particular circuit used in the lab session an alternative method for frequency step generation exists. This method consists of toggling the least significant bit of the feedback divider from N to N+1 to produce an equivalent PLL output to that which would be observed for a frequency step of the reference frequency. This action can be seen by remembering the relationship between in put and output frequencies is.

$$F_{out} = N \cdot F_{in}$$

Equation 3 **Relationship of output to input frequency for an integer N frequency synthesizer.**

Note that this method is the one that will be used in the following practical work, however it is generally only valid for frequency synthesizers that include a controllable feedback divider network.

Basic Board Set-up:

This section outlines the initial jumper and divider settings that have to be made before commencing the test.

Warning: Before commencing any of the tests ensure that:

- The initial board checks in section 1 have been carried out
- The information supplied in Appendix 1 has been read, and understood.

The diagram below shows the topside silk screen of the PLL test demonstrator board, the outlined numbered sections indicate areas of the circuit that are of importance in this practical session.

Figure 3Pll demonstrator board topside silkscreen.

With reference to figure 1 the table below explains initial set-up details for the particular test.

Jumper Block#	Associated components (Location)	Position details	Comments
1	J3 (Top) J1 (Bottom)	OFF ON	Isolates external reference.
2	U2 8way DIL Switch.	11101100 [1][2]	Divides the master oscillator by 20. Sets divided reference to 50KHz
3	U12 8way DIL Switch.	11101100 [1][2]	
4	J2	ON	Connects the PLL loop filter node to the VCO control input.
5	J4 (Bottom) J5 (Top)	ON OFF	
6	U8 8way DIL Switch.	11101100 [1][2]	Sets the PLL feedback divider ratio to 21.

Table 1 Initial Pll demonstrator board set-up.

Notes:
[1] 1 = Switch in the on position.
0 = Switch in the off position.
[2] This is set to give an initial overall PLL feedback divider ratio of 42 (remember that the VCO output signal passes through a high speed divide by two element before being fed into the lower speed adjustable feedback divider).

Comments on the board set-up

With reference to table 1 the following points apply to the PLL operation in this particular test set-up.

Test Hardware Physical set-up:

This section outlines the initial interconnection details for the external test equipment. The following figure illustrates the test pins that are used for this particular test.

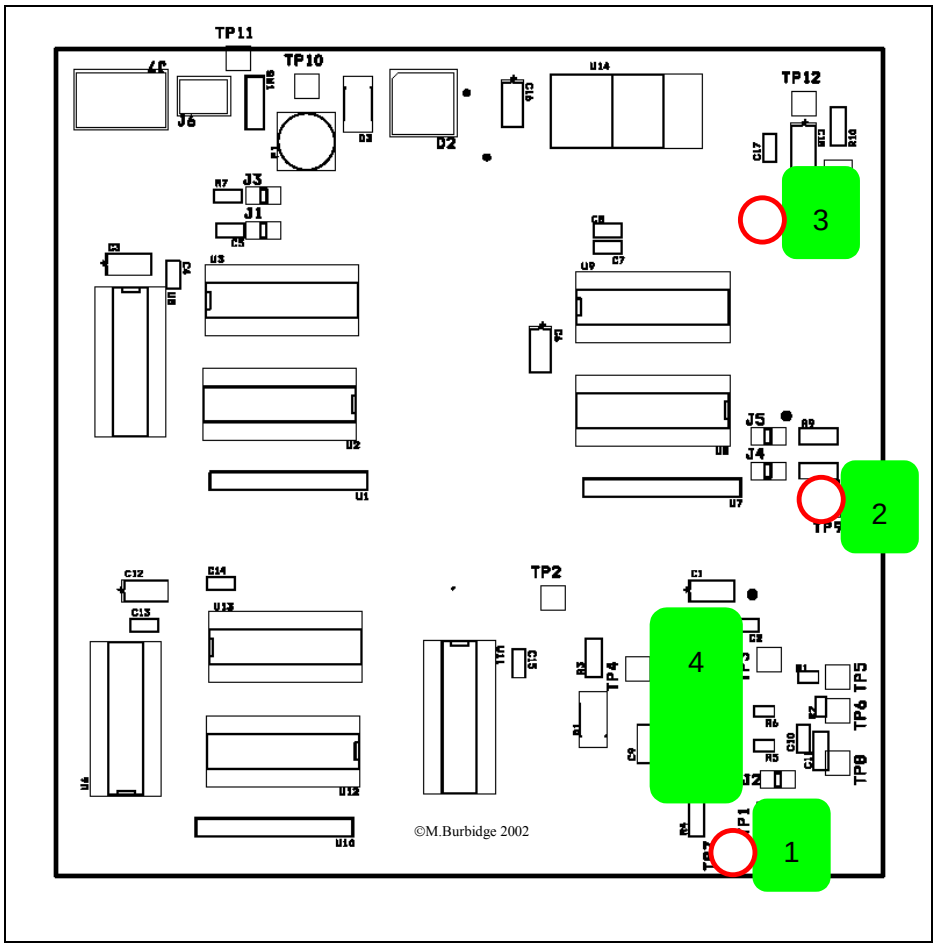

Figure 4Test pin and component details.

With reference to the above diagram the table below indicates the function of the test pins for this particular test.

Block#	Component / (Schematic Ref /PIN)	Test function
1	PLL (TP7)	Allows monitoring of the buffered loop filter voltage.
2	Test pin (TP9)	Allows monitoring of the toggle signal. This signal is useful for triggering the scope during the step response test.
3	Test pin (TP13)	Board ground connection.
4	PLL (pin 4)	PLL VCO output.

Table 2 Test pin function table.

With reference to table 2 and figure 2 the initial oscilloscope connections should be made as follows.

Oscilloscope settings:
Connect the channel 1 probe tip to point 1 (schematic TP7) in figure 4.
Connect the channel 2 probe tip to point 4 (schematic TP9) in figure 4.
Connect both of the earth clips to point 3 (schematic TP13) in figure 4.
Connect the digital channel 0 probe to pin 4 of the PLL (schematic U4).
The initial oscilloscope settings can be loaded from the file "QFILE_00" on floppy disk (or in the local directory *Instrument Files*) using the following buttons on the oscilloscope.
Save/Recall =>Recall =>From QFILE_00

After these connections have been made the board can be powered up.
If everything is working correctly an oscilloscope display similar to the one shown below should appear.

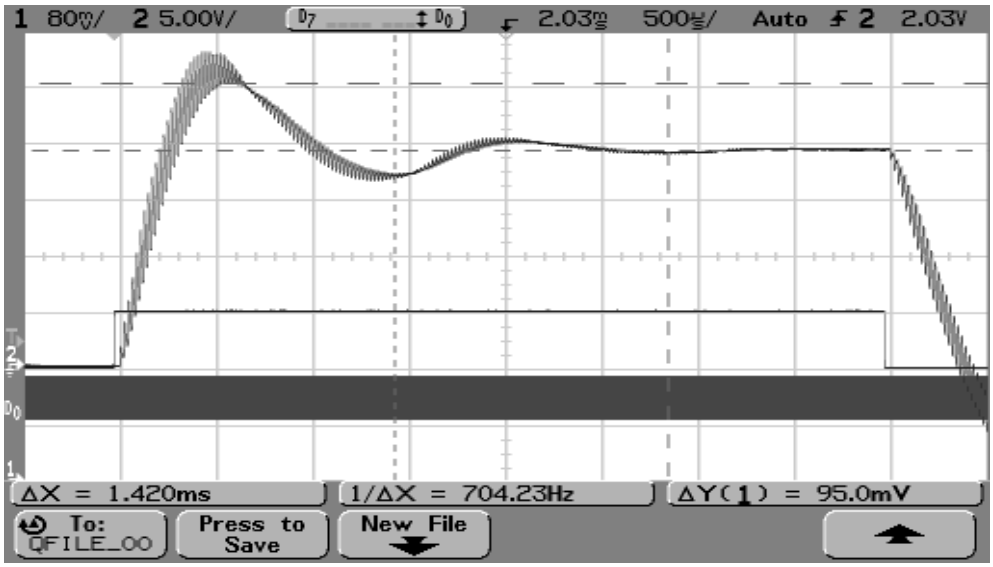

Figure 5Pll step response from N=21 to N=22 (2.1MHz => 2.2MHz).

The largest plot of figure 5 shows the step response of the PLL taken from the buffered loop filter node for a step from 2.1MHz to 2.2MHz. The middle plot shows the toggle signal, this signal is also used to trigger the oscilloscope. The lower plot shows the VCO output of the PLL. Note that changing the time base of the oscilloscope will allow observation of the full step from 2.2 to 2.1 MHz.

2.0 Step response measurement.

2.1 Step response for 2.1MHz to 2.2MHz.

Figure 6Scaling of oscilloscope display for measurement of peak frequency.

Questions

1) What are the values for peak overshoot (A1 figure 1), undershoot (A2 figure 1), and T.
2) What are the estimated the estimated frequencies for overshoot, undershoot and steady state conditions?
3) What is the approximate settling time of the PLL?
4) Estimate the natural frequency and damping factor from the response plots. How do the estimated values compare with the values calculated from the component values?

2.2 Step response for 2.9MHz to 3.0MHz

Switch off the board and change the feedback divider ration so that the step response is carried out for a frequency step of 2.9 to 3.0MHz.
Note that you may also have to adjust the toggle time so that the full transient response can be observed. As a starting point change the toggle period to about 24ms.
With these settings made power up the board and you should see a display similar to that shown in figure 5.

Questions
Try to carry out the same set of measurements as those outlined above. (number the answers from 5 to 8).

9) How does the response differ form the previous response?

Step response measurement; Answer Sheet 4:

Student Name:……

Date:……..

This sheet relates to any in text questions that were asked in this practical.
If response plots or post processing graphs were requested, please name them and attach them to this sheet.

Answer#	
1	
2	
3	
4	
5	
6	
7	
8	
9	

Technicians set-up notes and tutors details:

For this practical the equipment should initially be set up as outlined in section 1. In addition to the oscilloscope and power supply, the following equipment and software is required.

Hardware:

- RS232 lead to scope.
- Digital probes.

Software:

- Scope setting files => QFILE_00.* are loacted in the local instruments files folder. These files should be copied onto a floppy disk and distributed to the students.
- Agilent scope toolbar for Word.

Answers and further information:

- Details of the switch settings in the AnswerSheets folder (switch settings are also given in appendix 1.
- Sample answers to the questions are provided in the local AnswerSheets folder.