PLL Tests
Simulation Models and Equations.

Author Details:

Dr. Martin John Burbidge
Lancashire
United Kingdom

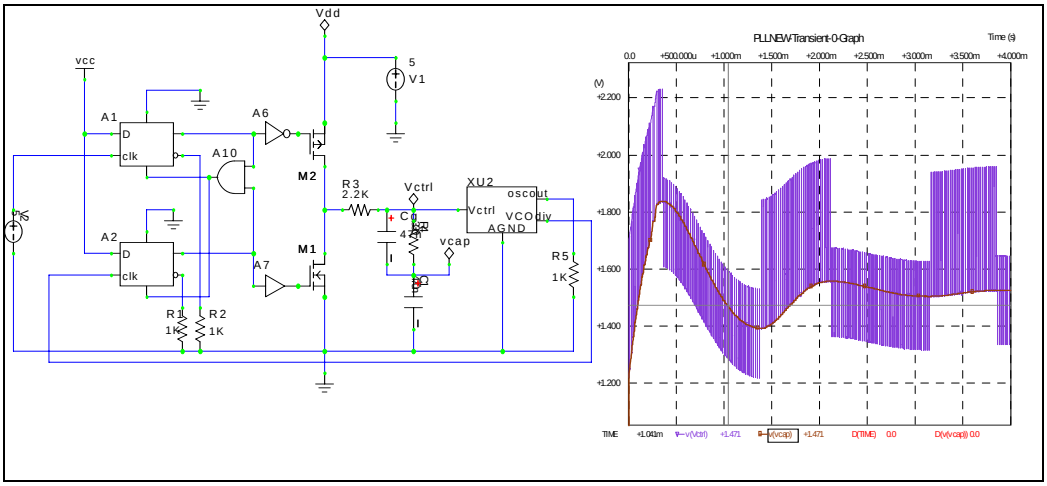
Tel: +44 (0)1524 825064

Email: martin@mjb-rfelectronics-synthesis.com

Document Priority: Normal, primary simulation results.
Associated Material: {1}, All PLL test practical module documentation.
Required software: Matlab 5.3 (or Gnu Octave 2.3.1), B2SPICE LITE 4.1.
Note: that further details are given in the software details section below.
Note: this document is for review purposes only. Some items have been deliberately removed

Purpose:

The material in this document contains examples and descriptions of simulation models that map to the physical PLL hardware used in the PLL test practical sessions. It is expected that the models explained in this section be investigated prior to carrying out the practical exercises. The document also includes relevant equations for the practical sessions and the simulations.



Contents

Section Contents

Figures, Tables and Equations

Preface – Software requirements and model locations:

Behavioural Spice and Xspice models:

All of the spice models for this course will run under a software package called B2SPICE A/D v4. All of the models have been adapted from original models so that the can be run in the LITE version of the software. This can be downloaded from the following location

http://www.beigebag.com

The simulation files for this module are located in the local directory "PLLSPICE".
The models are simulated by opening the respective circuit and selecting the *Simulation => run simulation* option from the tool bar.

Analytical models:

Analytical models are provided for both MATLAB and GNU Octave (a matlab clone). The MATLAB files will work on the student version of the software.
The GNU Octave software can be downloaded from:

http://www.octave.org/

The simulation files are located in the local directory PLLMATLAB.
Details are provided in the files for any conversions that may be required to run them in the OCTAVE environment.

To compile and run the models place them in the following directories.
Matlab install DIR \ WORK. For the MATLAB files.
GNU OCTAVE install DIR \ usr \ local \ share\ octave \ 2.1.31 \ m
For the OCTAVE files

1.0 Introduction:

Aims:

The primary aim of the material in this section is to allow the student to experiment with behavioural and analytical simulations of phase locked loops. It is expected that the student read the material in this section before carrying out the practical exercises. The main focus of the material is to allow the student to substantiate their understanding through practical examples.

Objectives:

After completing this module the student should be able to.

- ✓ Understand the Spice simulation models and relate them to the physical hardware.
- ✓ Have a basic understanding of the standard frequency-step and transfer function response plots.

Module Overview:

The purpose of this module is to provide the student with behavioural and analytical models that correspond to material included in the practical sessions. Phase locked loop simulation models are investigated with reference to the practical course material. This is so that the student can gain some familiarity with the test methods prior to attending the practical element of the course. The material in this module is also used to summarise the key equations relating to the course. An overview of the contents of this module is provided below.

- Spice PLL model and explanation and general equations.
- Standard analytical models for frequency step response and transfer function response.
- Simulations of various PLL blocks including.
  - Phase detector and loop filter.
  - VCO (Voltage controlled oscillator).
- Spice simulation for step response.
- Spice simulation for phase transfer response.

2.0 Overview of the Spice PLL model.

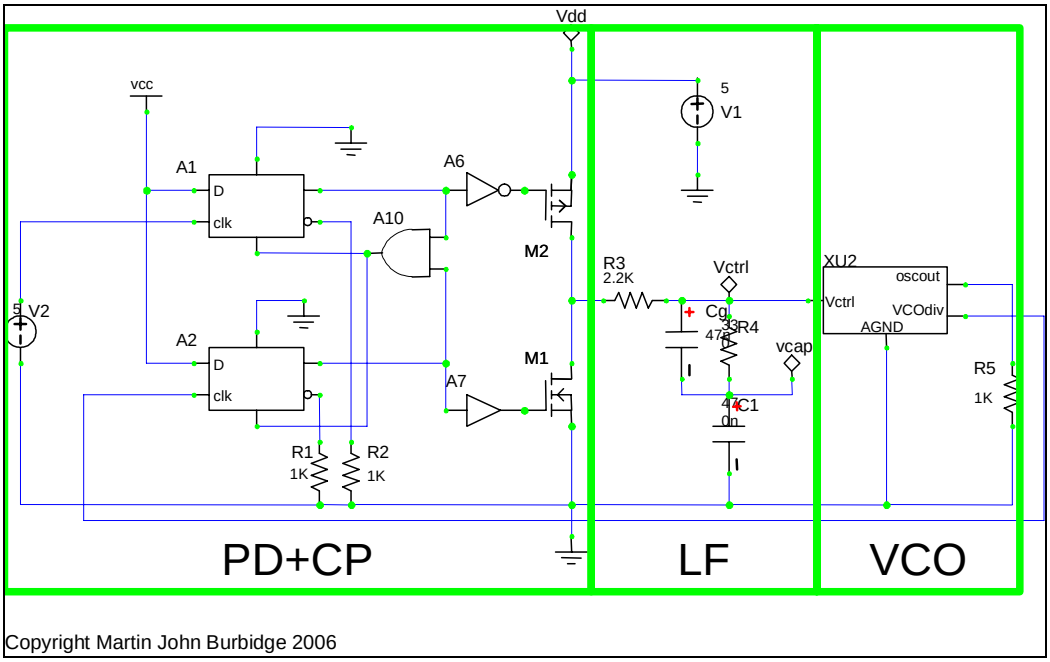


Figure 1 Spice Phase locked loop simulation model.

Note: It will be useful to have the "MainPLL.ckt" file open for reference whilst reading the explanation below.

The circuitry depicted in figure 1 represents a mixed signal model of the 74HCT4046 Phase locked loop that is used for the practical exercises. The key elements of the simulation model are explained below along with their respective parameters. The information in this section is only intended to provide a brief overview of the key PLL sub sections, further information on PLL operation is provided in {1, 2, 3}.

1) **PD+CP:** This part of the circuit models the **Phase detector** and **Charge-Pump** respectively.
   a. **Phase Detector:** The purpose of the phase detector is to produce correction signals at its outputs (see M2 and M1) that are proportional to the difference at its inputs (see A1 clk and A2 clk). Note that the phase detector in this circuit only operates on rising edges of the input signals. Also this type of phase detector has a detection range of $\pm 2\pi$ (360°).
   b. **CP:** The charge pump circuit converts the outputs from the phase detector into voltage signals that are directly proportional to the phase difference on the PLL inputs.

Note that the voltage source V1 is used to generate the phase locked loop reference signal. The associated gain of the phase detector and charge pump together is usually expressed as K_d where:

$$K_d = \frac{V_{cp\max} - V_{cp\min}}{4\pi}$$

Equation 1 Phase detector and charge pump gain.

Where: V_{cpmax} is the maximum voltage the charge pump output transistors can supply before saturation and V_{cpmin} is the minimum voltage the charge pump output transistors can supply.

For the particular circuit we are interested in the output of the phase detector is approximated as.
0.4 v/r (volts per radian)
This value is taken from the data sheet for the 74HCT4046AN PLL which is supplied in the "Appendix1" folder.
Note: For this particular type of phase detector the gain is non linear. As we have a voltage source driving an RC network (the loop filter circuit) the output has an exponential relationship. This means that the gain will change over the full operational range of the phase detector.

2) **LF: Loop filter:** The basic function of the loop filter is to provide a filtering action on the PLL input signal and other higher frequency terms in the signal that are produced due to the phase detector action. In the steady (or locked) state the loop filter output should be a stable voltage that is suitable for the control of the VCO.
With reference to the simulation model, the transfer function of the loop filter for this particular PLL is provided below.

$$F(s) = \frac{1+\tau_2}{s(\tau_1+\tau_2)}$$

Equation 2 Loop filter transfer function.

Where:

$\tau_1 = R3 \cdot C1$ (s) (See note below)

Equation 3 Calculation of t1

And,

$\tau_2 = R4 \cdot C1$ (s) (See note below)

Equation 4 Calculation of t2

Note that for this particular circuit the schematic designators are used for the component values in equation 2. However, in some of the analytical models and definitions in later parts of the text R3 may be designated as R1 and R4 may be designated as R2.

Also: A small deglitching capacitor is included Cg is included in the loop filter network. For the purpose of analysis and analytical models used in later sections its action upon coarse overall PLL response can be omitted.

3) **VCO: Voltage Controlled Oscillator:** The purpose of the VCO is to produce an output signal whose frequency is proportional to its input voltage.
Gain of the VCO is a measure of how much the output frequency of the VCO changes with respect to a change in input voltage i.e.

$$K_{vco} = \frac{\Delta\omega}{\Delta V} \text{ (rps/v) (radians per second per volt)}$$

Equation 5 VCO gain equation

Note: that K_{vco} is often given in units of r/s/v, however in certain circumstances it is better to give the value in terms of Hz / v. The form of equation 5 can be converted to Hz/v by dividing by 2π.

4) **Loop divider:** It is not shown in the simulation model, but most of the CP-PLL synthesisers that are in use include some form of feedback divider network. The feedback network usually changes the VCO frequency to a lower frequency before it is fed back to phase detector input for comparison with the reference signal. Assuming that all the other parameters are set up correctly, inclusion of a feedback divider allow the PLL to generate and output signal that is an integer multiple of the reference signal supplied to the PLL i.e.

$$F_{out} = N \cdot F_{in} \text{ (Hz)}$$

Equation 6 Relationship between PLL output frequency and input frequency for integer divider ratio.

Where: Fout is the frequency of the PLL output signal, Fin is the frequency of the PLL input signal or reference signal, and N is the value of the divider.

The actual PLL circuit used in the practical sessions contains a feedback divider constructed from a digital counter. However, in the simulation model the division ratio is incorporated directly into the VCO description.

Where: K_{vco} is the VCO gain, K_d is the phase detector gain and ωn is the natural frequency of the PLL system.

For the circuit in question ω_n and ζ can be defined as follows:

$$\omega_n = \sqrt{\frac{K_O K_{PD}}{N(\tau_1 + \tau_2)}}$$

Equation 7 Derivation of natural frequency from circuit parameters.

and

$$\zeta = \frac{\omega_n \tau_2}{2}$$

Equation 8 Derivation of damping factor from circuit parameters

Note that a **MATLAB** file **WDComp_est** that calculates equations 10 and 11 is included in the local Matlab directory.
The natural frequency and damping of the loop will control the transient response of the loop (including settling time and overshoot) and will also have direct control over the loop bandwidth. More information about the natural frequency and damping is provided in practical modules 3 and 4, which cover phase transfer function monitoring, and frequency step response monitoring respectively.

3.0 Normalised analytical response plots.

In many situations the initial part of the design phase starts with a specification for desired final system performance. With a PLL, typical design issues centre on bandwidth and transient response of the final system when it is subjected to certain inputs. Commonly used inputs that can allow frequency and transient response to be calculated are sinusoidal frequency modulation and frequency steps respectively. Inputs such as the ones mentioned are also relatively easy to generate in reality, and can thus be used to evaluate the performance of the final system.

It is common to find normalised frequency response plots and transient response plots of systems reproduced in PLL and control system texts. The response plots are generated using equations 7 and 9.

3.1 Normalised Frequency response plot.

The plot of magnitude and phase response of the output signal of the PLL when it is subjected to an increasing input modulation frequency is shown below.

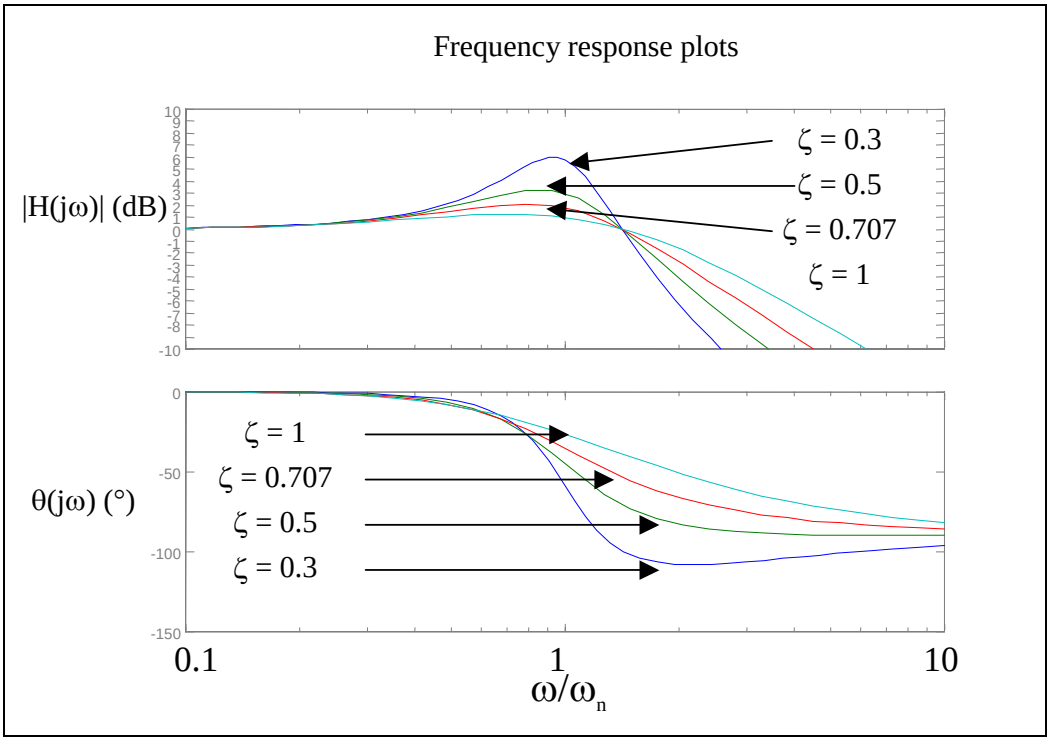


Figure 2Frequency response plots for PLL system.

The plots shown in figure 2 were created in MATLAB using equation 7.
A copy of the program listing that will generate normalised plots for damping factors is included in the local Matlab and Octave directories as PLLTransfer.m.
Note that the transfer function can also be plotted manually by making the substitution.

$$s = j\omega$$

Equation 9 Substitution for manual transfer function plotting.

Into equation 7.

3.2 Normalised Frequency step response plots.

The following figures show normalised PLL step response plots when the PLL is subjected to an input frequency step.
Plots are derived from equation 9.

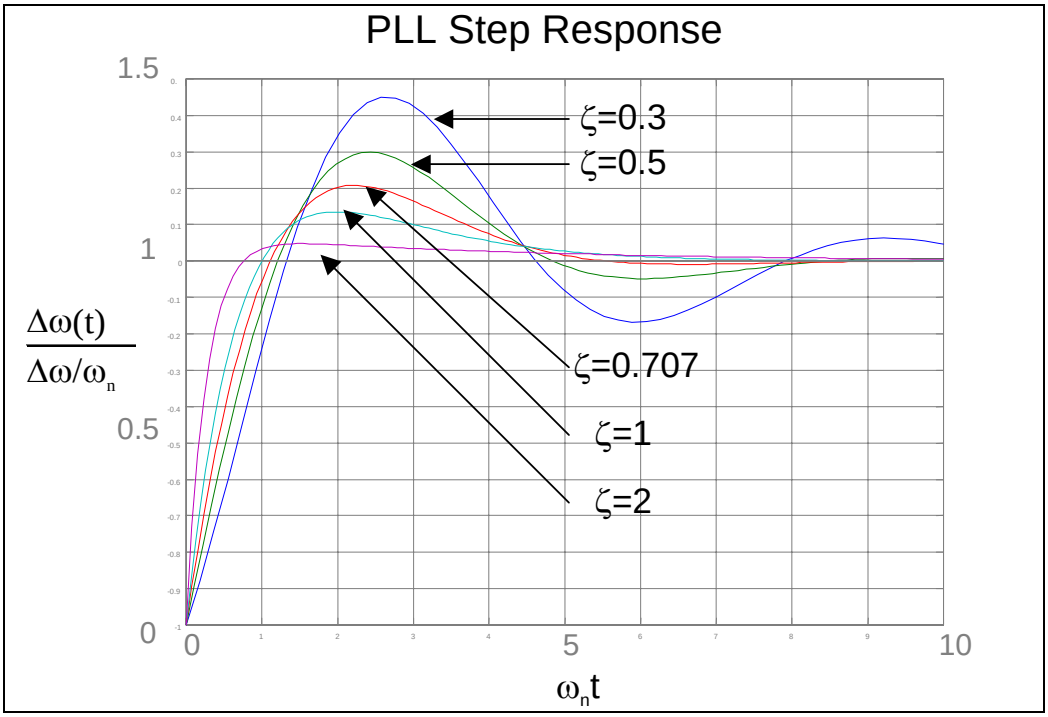


Figure 3Step response plots for input frequency step.

Both of the plots shown in figures 2 and 3 may be used to aid estimation of component values.
For instance a final system may be specified to have the following characteristics.

- Settling time <= 1ms to 5% of the steady state value.
- Overshoot < 30% over the steady state value.

If we initially choose the plot for ζ = 0.707 from figure 3 the overshoot is approximately 20% (from the graph) this will give a suitable safety margin.
Then inspection of the graph shows that the selected curve has settled to within 5% for:

$\omega_n t = 8$

Therefore the required value for ω_n is

$$\omega n = 8/t = 8/1ms = 8kr/s$$

Equation 10 Example calculation for natural frequency from step response graphs

The estimated values for the natural frequency and damping can then be used in conjunction with equations 10 and 11 to allow initial system design to be carried out. Note that there are worked examples of PLL design in the 74HCT4046AN PLL data sheet {4} and {1}.

It is important to mention that when measurements are being taken from phase locked loops it is often more convenient to use simple formulas for the estimation of the natural frequency and damping. Module 4 of the practical sessions includes example equations for phase locked loop measurement.

MATLAB code for the equations is included in the local MATLAB directory as **WD_est.m**

4.0 Spice simulation models.

There are various Spice simulation models included in the local directory PLLspice. These simulation files are used to model the PLL that is included on the PLL demonstrator board used in the practical sessions. The simulation files are primarily included to allow you to investigate the PLL operation relating to specific tests, before commencing any of the practical work. Specific tests will include step response and phase transfer function monitoring. In addition, this section will cover simple simulations for various parts of the PLL including the Phase frequency detector, loop filter and the VCO model.

4.1 VCO model and test simulation. (Practical module 2)

The schematic for the model of the VCO with accompanying operational notes is shown in figure 4.

Figure 4simple behavioural VCO descriptions.

A description of the VCO model is provided with the associated circuit file **VCOTest.ckt** that is located in the local folder **PLLspice.**

The circuit file is ready to run in the simulation software. If you open the file and
Select => Toolbar => simulation =>run simulations
After a certain amount of time (approx 30s) you should see the following display.

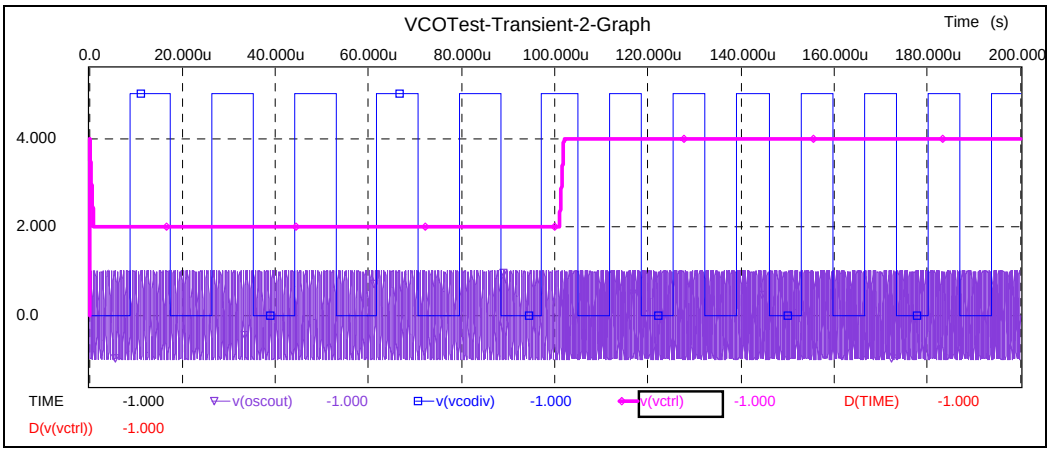


Figure 5Output responses for the VCO test.

The display of figure 5 shows the divided VCO output (blue high frequency square wave), the VCO control signal (pink square wave), and the high frequency oscillator output (at the bottom of the graph).
Various options are available in the
Toolbar => edit=> drop down menu.
It should be possible to use the cursor options to measure the VCO output frequency for the different control voltages.
You can also display further plots or modify plots by right clicking in the plot window and selecting the "*Edit Plots" option.*

4.2 PFD Charge pump and loop filter simulation.

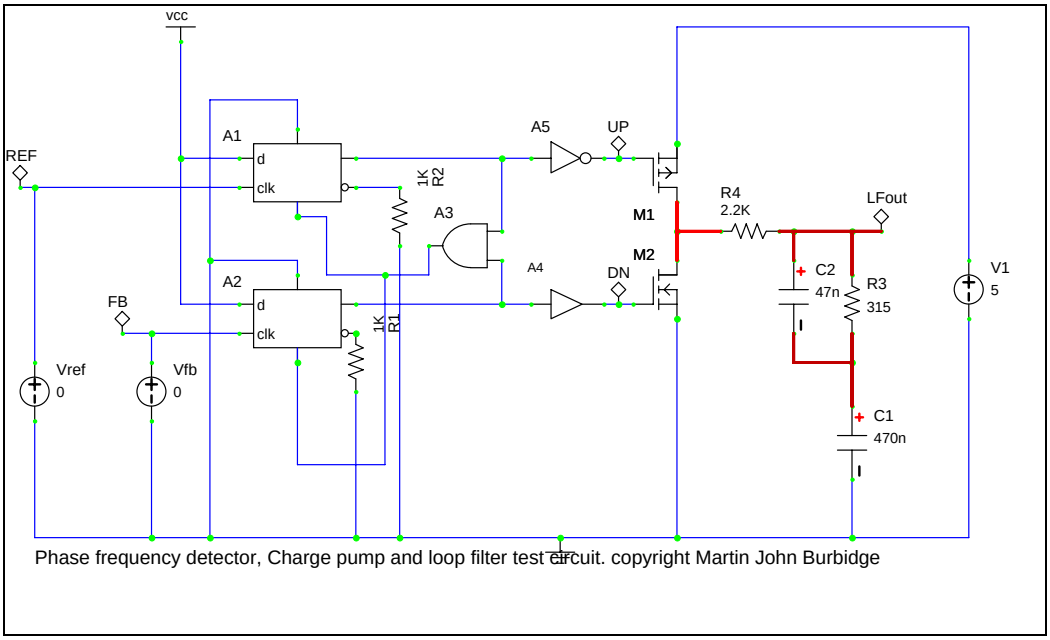


Figure 6 Phase frequency detector, charge pump, and loop filter test circuit.

The circuit shown in figure 6 is used to simulate the operation of the phase frequency detector, charge pump and loop filter circuitry contained in the PLL. Experimentation

with the simulations will provide valuable insight in to the operation of the various PLL sub-blocks.
The circuit file **PFDCPLF.ckt** is located in the local folder **PLLspice.**

The circuit file is ready to run in the simulation software. If you open the file and
Select => Toolbar => simulation =>run simulations
After a certain amount of time (approx 30s) you should see the following display.

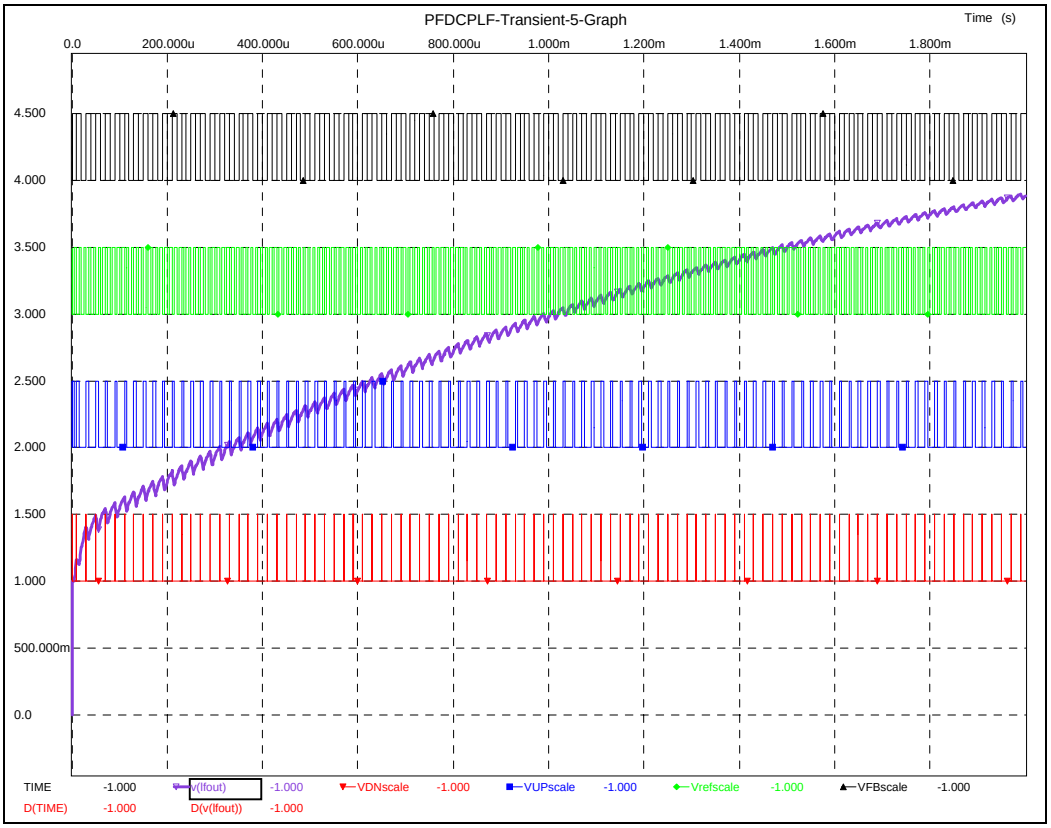


Figure 7 Example outputs for the PFD, CP and LF simulations.

In figure 7, the plots show the following outputs from the circuit:

- **Diagonal Plot:** This plot shows the output of the loop filter node over time. Note that in this case the loop filter voltage is increasing. The increase is due to the way the inputs to the PFD are set up (see below). Also note that the output of the loop filter node is non-linear. (See section 2 also).
- **Horizontal plots: Described from bottom to top.**
  - 1) Down pulses from the output of the phase frequency detector DN pin. These pulses control the operation of transistor M1.
  - 2) Up pulses form the output of the phase frequency detector UP pin. These pulses control the operation of transistor M2.
  - 3) PFD reference signal at 100KHz. Parameters can be investigated by double clicking on Vref in the circuit.
  - 4) PFD Feedback signal at 50KHz. Parameters can be investigated by double clicking on Vfb in the circuit.

Note: that the horizontal plots are scaled versions of the original signals. The plots were scaled to allow them to be viewed in one window. The original un-scaled signals would have a voltage of 0 to 5 volts.

To further investigate the operation of the forward path PLL components it will be useful to change the values of the input signals as follows:

- Feedback frequency twice the reference frequency.
- Feedback frequency and Reference frequency and phase the same.
- Feedback frequency and reference frequency the same but with different phases. Note that this can easily be achieved by changing the parameter Td in the voltage source set-up dialogue.

4.3 PLL step response simulation. (Practical module 4)

The information in this section concerns PLL step response tests and relates to material provided in module 4. It will be useful to read the associated information contained in section 4.

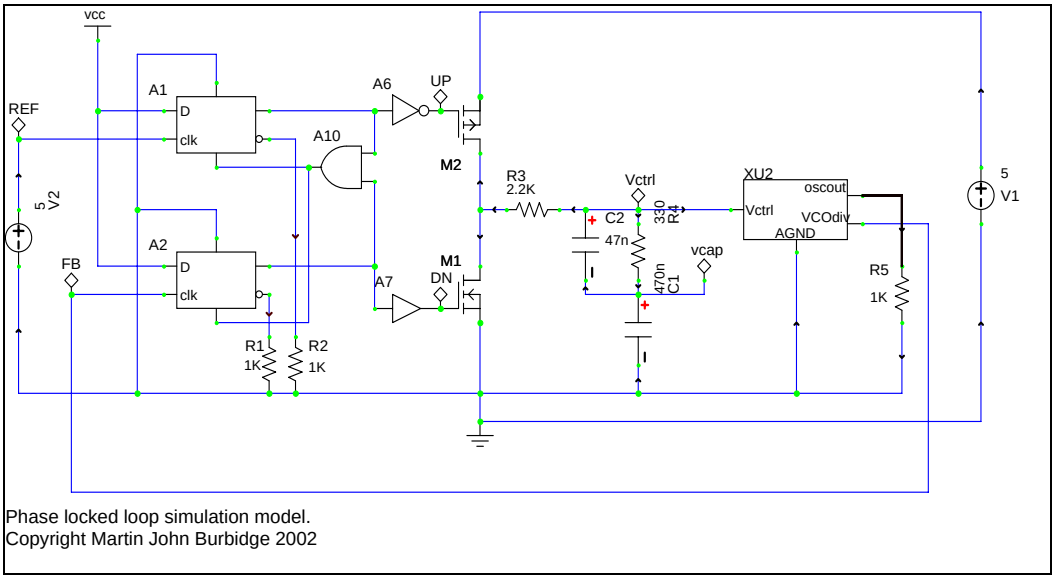


Figure 8 **Simulation model for step response test.**

The circuit shown in figure 8 is used for the simulation of the step response of the PLL for a change in the feedback divider between ratios of 40 to 42. The reference frequency of the PLL is 50KHz so the process effectively produces a step in the PLL output between 2MHz and 2.1 MHz (see equation 6 also).
The loop filter component values of the circuit are the same as used in the real circuit and it will be useful to estimate the damping factor and natural frequency for comparison to later plots (use equations 10 and 11 and N = 41). Note: that it is not necessary to include the deglitching capacitor in the equations (C2 figure 8).

The circuit file **MainPLL.ckt** is located in the local folder **PLLspice.**

The circuit file is ready to run in the simulation software. If you open the file and
Select => Toolbar => simulation =>run simulations
After a certain amount of time (approx 2minutes) you should see a display similar to the following.

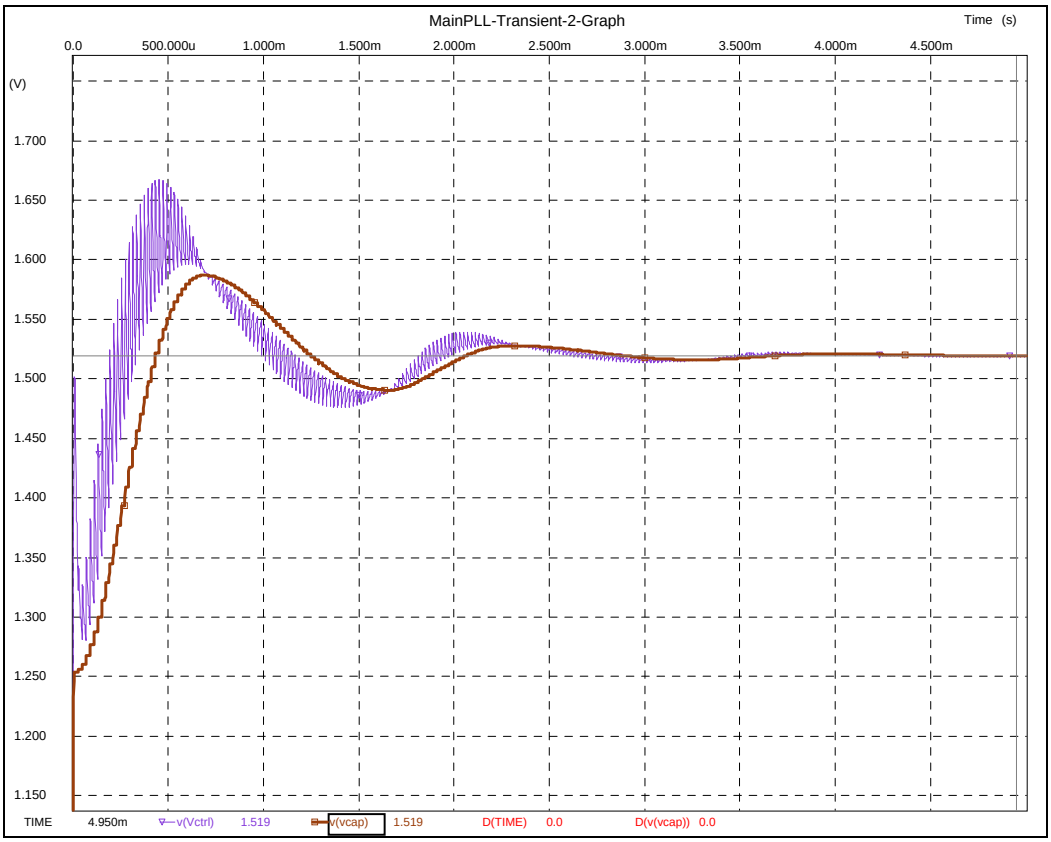


Figure 9Simulation plot for step response.

4.3 PLL transfer function simulation. (Practical Module 3)

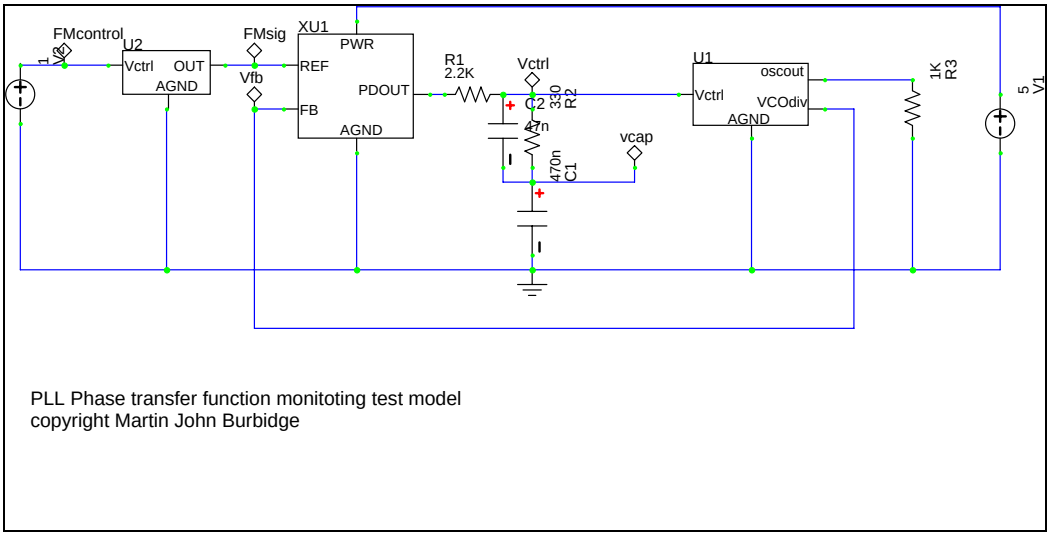


Figure 10 Pll phase transfer function simulation model.

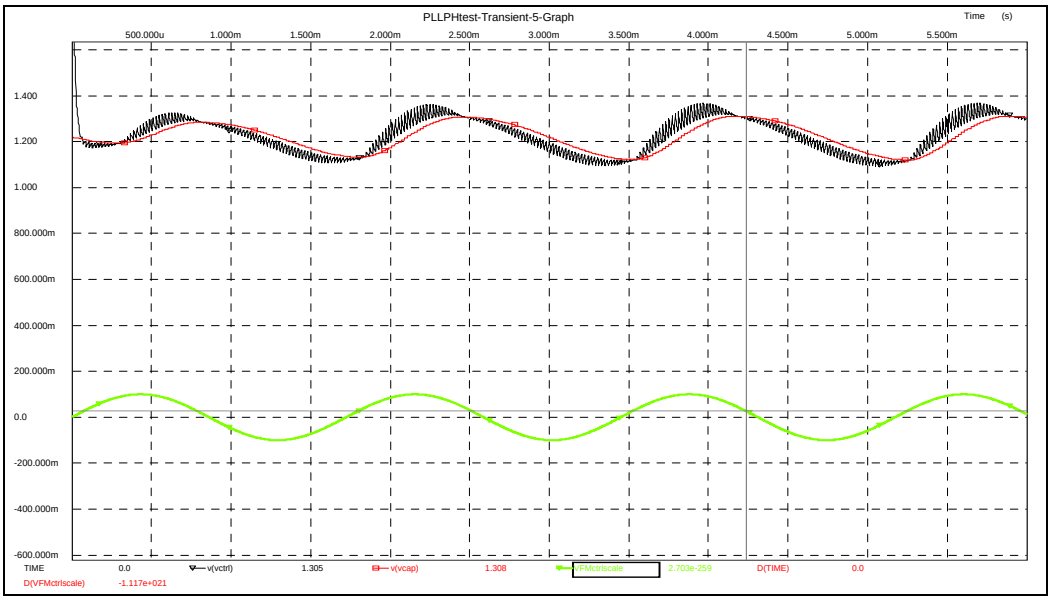


Figure 11 PLL phase transfer plots.

In the plots of figure 11 the green trace shows a scaled version of the FM control input to the PLL, the black trace is the loop filter control voltage, and the red trace is the voltage on the main loop filter capacitor.

You can use the cursors to measure the peak-to-peak output of the loop filter capacitor voltage and the time difference between the peak of the input signal and the peak of the loop filter response. The measured values can then be used to ascertain the peaking and phase delay of the output signal, with the techniques shown module 4.
Note that the measurements should be taken after the PLL has settled, i.e. after about 3.5ms in the plot.

You may want to change the modulation frequency and make further measurements to produce a coarse plot of the phase transfer function similar to the one that will be carried out in module 4.

Simulation files and code listing locations

Item	Type	Local Folder Location
WD_est.m	Matlab code	MATLAB
PLLTransfer.m	“”	“”
PLLPFstep1.m	“”	“”
WDComp_est	“”	“”
VCOTest.ckt	Spice circuit	PLLspice
PFDCPLF.ckt	“”	“”
MainPLL.ckt	“”	“”
PLLPHtest.ckt	“”	“”

Table 1 Simulation files and code listing locations.