Simple Frequency Counting Techniques for Analysis of VCO / CP-PLL Coupled Noise Sensitivity in Fully Embedded CP-PLLs

Martin John Burbidge
Lancaster University, UK.
email: m.burbidge@lancaster.ac.uk

Abstract

Fully embedded CMOS CP-PLLs (Charge-Pump Phase-locked loops) systems are currently used in a variety of SoC (System on Chip) applications. Often the key CP-PLL performance metrics are stated in terms of spectral purity of the output signal. Spectral purity can be severely degraded due to forward path faults or externally coupled noise. A correctly designed fully embedded CP-PLL system can be sensitive to particular forward path leakage faults that could be introduced during manufacture. In addition, the CP-PLL structures and particularly the VCO (Voltage controlled oscillator) can be critically sensitive to coupling of externally generated supply and substrate noise. Methods for detection and analysis of key forward path degradation mechanisms have been reported previously. The techniques can provide some indication of important VCO parameters , however, no monitoring of externally coupled noise is carried out. This paper presents initial investigations into use of simple frequency counting methods for detection of externally coupled noise into the CP-PLLs VCO structures.

Keywords: PLL, CP-PLL, Jitter, Deterministic Jitter, Voltage controlled oscillator, coupled noise immunity.

1. Introduction.

Fully embedded CMOS CP-PLLs (Charge-Pump Phase-locked loops) are currently used in a variety of SoC (System on Chip) frequency synthesis applications. Often the key CP-PLL performance metrics are stated in terms of spectral purity of the output signal or jitter of the output signal. Unfortunately, even in a characterisation environment it can be difficult to directly assess the quality of the output signal in these terms. During characterisation, luxuries, such as, specialised test equipment, test fixtures, test chips, additional on chip access buffers and prolonged test times are often permitted. However, in a production test environment measurement problems can become exacerbated and direct measurement of the spectral purity of the output signal is often not an option. A correctly designed fully embedded CP-PLL system can be sensitive to particular forward path leakage faults or deviations that can be introduced during manufacture. Typical excessive forward path deviations will lead to deterministic direct modulation of the VCO (Voltage Controlled Oscillator) control terminal. This modulation manifests itself as deterministic properties in the output spectrum and the associated jitter of the system. In addition, the output spectrum of the CP-PLL can be severely degraded due to externally coupled noise from the chip substrate or power supply. For digital SoC, significant noise generation can occur due to digital switching activity [1][2]. If this noise is coupled into the CP-PLL structures and particularly the oscillator structure, it can cause direct modulation of the CP-PLL output signal spectrum. To obtain the best rejection of externally coupled noise, a commonly used architecture for embedded CMOS oscillators is the differential current starved ring oscillator [3]. However, VCO structures can be particularly sensitive to supply coupled noise; therefore, much of the design effort of the CP-PLL is focussed towards decoupling.

Coupled noise can raise the phase noise spectrum of the CP-PLL. In addition, deterministic noise spurs can appear. In consequence, it is essential that the CP-PLL output signal purity is investigated when other on chip circuitry is active. In [4][5] experiments were carried out with respect to detection of typical forward path leakage faults using simple open loop "Ramp" methods. In addition, the relationship between forward path open loop deviation and output spectrum degradation was investigated. The techniques explained could be used to

yield some important information about oscillator operation, such as gain, linearity, and lock range. However, the oscillator structure was not evaluated for externally coupled noise. This paper extends the work from [4] [5] and provides initial investigation into the possible use of similar circuitry for the verification of coupled noise immunity. The attempt was initially made to investigate techniques that could be used to force the CP-PLL into an open loop mode, thereby sensitizing the oscillator structures to externally coupled noise. The resultant frequency deviations of the oscillator are then monitored using frequency counting techniques. A similar technique for high-resolution measurement of on chip supply noise using an on chip open loop VCO and associated sampling system was proposed in [2]. However, in this paper the technique is initially investigated and proposed as an alternative to evaluating the CP-PLL coupled noise immunity.

The paper presents the following information.
Section 2, Explains the behavioural CP-PLL model and oscillator circuit topology used for the experiments. In addition, an indication of values used for noise coupling is provided.
Section 3, provides an explanation of a possible test set up procedure, and outlines key features of the proposed measurement procedure.
Section 4, Provides an indication and analysis of initial simulated measurement results.
Finally, section 5 provides conclusions and indicates areas for further work.

2. CP-PLL, sensitivity issues, models Voltage Controlled Oscillator structure and noise injection.

Experiments were carried out using a behavioural model of an integer-N CP-PLL. The VCO structure was described at the transistor level. The following subsections explain the model and circuit details.

2.1. CP-PLL model behavioural section.

Figure1 Illustrates the block level diagram for the PLL macro model.

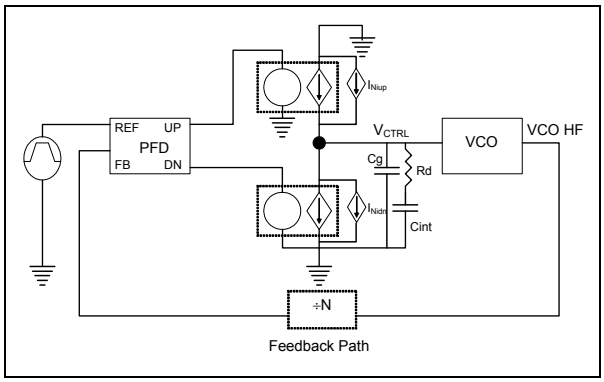

Figure 1 CP-PLL Behavioural model.

The key elements of the model are now described from left to right.

The reference signal for the PLL is currently modelled using a SPICE pulse source. For the analyses, it is assumed that a clean reference source is available.

The PFD is modelled as an edge sensitive type IV phase and frequency detector and is described using VHDL primitives.

The charge pump sources are modelled using voltage controlled current sources.

The loop filter components are standard SPICE elements. C_g is the deglitching capacitor that removes high frequency transients from the charge pump switching action. R_d is the loop filter-damping resistor. C_{int} is the main loop filter capacitor.

The VCO structure is described at the transistor level and is a four-stage fully differential ring oscillator topology. Not shown in the model is a single ended to differential conversion stage that is used to convert the loop filter voltage Vctrl to the differential inputs of the VCO control terminals. Further details of the VCO circuit are provided in the following subsection.

The feedback divider structure is modelled behaviourally. All of the behavioural models are described using C style algorithms for use in the SMASH™ simulation package.

2.2. VCO circuit topology.

The VCO circuit model was developed at the transistor level using 0.35 um BSIM3V3 transistor models. The circuit topology chosen was a four-stage differential ring oscillator structure. This topology was chosen because it should be more insensitive to supply coupled noise. This seems to be the case when considering common mode noise coupled to the VCO control terminals and feedback paths. The basic four-stage ring oscillator schematic is shown in figure 2.

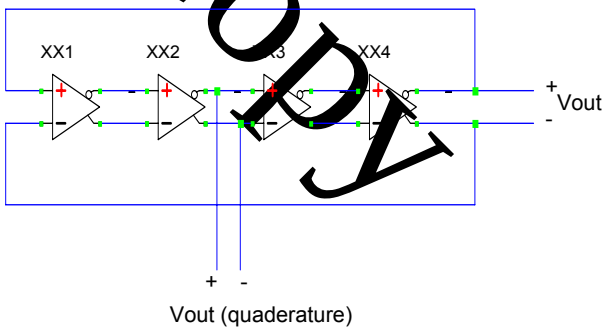

Figure 2 4-stage differential oscillator structure.

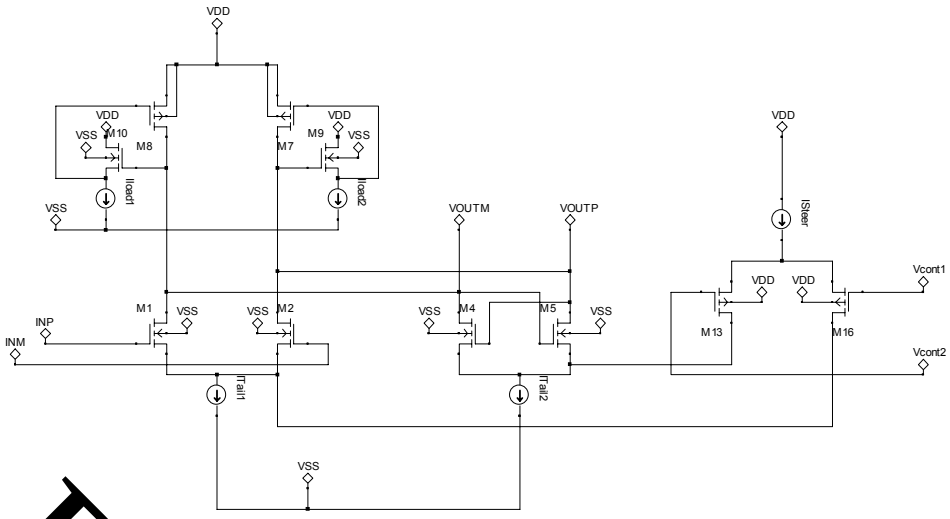

Figure 3 Differential Delay cell structure.

In figure 2, the individual delay elements (XX1 to XX4) are constructed from voltage controlled differential delay elements. The schematic of an individual delay stage is shown in figure 3. The circuit is based upon a differential delay stage architecture taken from [3]. The transistor W/L ratios were initially scaled so that the oscillator produced a 300MHz output signal for a 1.446-volt differential control voltage and a 3-volt supply voltage. In addition, the oscillator gain was found to be relatively linear over a 250MHz to 350MHz range. The delay cells were initially designed and characterised using Agilent ADS. Then identical cells were netlisted for inclusion in the SMASH™ simulation package with the behavioural models.

2.3. CP-PLL model parameters.

The estimated parameters for the CP-PLL loop system are provided in table 1.

Design Parameters	Comments	Value
Ref	Reference Frequency	10 MHz
Division Ratio	Feedback divider ratio.	30
Output Frequency	Final PLL output frequency.	300 MHz @ Vctrl=1.446V
Ipump	Charge pump current magnitude	10 uA
Kvco	VCO gain MHz/V	268 MHz /V
Cint	Main filter capacitor.	100 pF
Cg	Deglitching capacitor.	10 pF
Rd	Damping resistor.	25 Kohm
Derived Parameters		
ω_n	Natural Frequency	945.163 Krps 150.427 KHz
ζ	Damping Factor	1.184
B_L	Noise bandwidth (one sided)	658.312 Krps 104.733 KHz

Table 1 CP-PLL parameters.

Equations for derived parameters can be found in [3] [6] [7].

Important derived parameters of table 1 relate to the loop bandwidth (B_L), the natural frequency (ω_n)and the damping factor (ζ). These parameters will define how the CP-PLL will react to signals within the loop bandwidth. In general, the CP-PLL will track deterministic signals below ω_n and suppress signals outside this range. In addition, depending on the value of ζ signals may be slightly amplified at ω_n. Therefore, deterministic externally coupled noise components that lie within the loop bandwidth will undergo less suppression than components outside the loop bandwidth.

2.4. Initial supply noise injection.

For the experiments shown in later sections, known deterministic supply noise of different frequencies was injected into the oscillator Vdd connection. Representative amplitudes for the supply noise were taken from [8] for a PLCC-68 pin package. Amplitudes used, relate to analogue Vdd noise and assume that the analogue circuitry has separate Vdd and Gnd connections. Vdd values were initially chosen as they are lower than the values stated for ground noise. The lowest value of noise was chosen in conjunction with error free circuits to attempt to highlight the sensitivity of the detection process. In the experiments, composite supply noise was emulated by the summation of continuous square waveforms at specific frequencies. Pulse waves were chosen to provide a better representation of noise that could be introduced from digital switching activity of other on-chip circuitry. Values are provided in table 2.

Pk-Pk noise	103mV					
Supply voltage	3V					
Composite square wave frequencies	10K	100K	1M	10M	100M	600M
1) Amplitudes near to loop BW	17.17	17.17	17.17	17.17	17.17	17.17
2) Amplitudes above loop bandwidth	N/A	N/A	N/A	34.33	34.33	34.33

Table 2 Noise frequencies and amplitudes.

In table 2 all amplitudes are in milli-volts and represent peak to peak values. All frequencies are in Hz

In the table, the shaded columns indicate frequency components that are close to, or within the PLL loop bandwidth. Experiments ware carried out for externally coupled noise, including and excluding these frequency components. In addition, externally coupled random noise of 103mV was injected into the closed loop CP-PLL. In a real measurement situation, it is expected that the noise would be generated due to activity of other on-chip circuitry [8].

3. Test approach details.

The proposed evaluation approach initially relied upon sensitization of the CP-PLLs VCO structures to any supply coupled noise, in conjunction with repetitive frequency counts of the VCOs output frequency. Sensitization of the VCO is accomplished by opening the CP-PLL loop after the lock condition has occurred and applying a stable control voltage to the VCO control input. Measurement of the open loop VCO as appose to the closed loop CP-PLL is preferred. This is due to the fact that to produce a stable output signal the CP-PLL will attempt to average any perturbations on the oscillator output over many cycles of the reference waveform. Thus, for a PLL operating in the closed loop condition, a corresponding measurement of the output signal averaged over many cycles (i.e. a frequency count) will produce a correct frequency value. However, if the CP-PLL and hence the VCO is in the open loop condition when the measurements are made the compensation cannot occur and the VCO output frequency will be wholly dependant upon its control voltage and effects due to coupled noise.

Open loop CP-PLL techniques presented in [4] [5] were used to assess leakage in the forward path components of the CP-PLL. In the approach, the loop was opened by breaking the feedback path and applying identical signals to the CP-PLLs Phase and frequency detector inputs. This procedure was carried out after the locked condition had occurred. The approach is illustrated in figure 4.

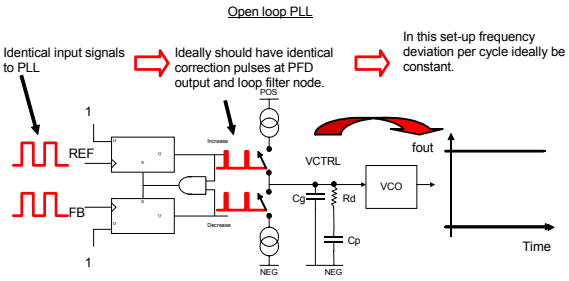

Figure 4 Open loop CP-PLL operation.

For a correctly operating CP-PLL the loop filters control voltage and hence the VCO output frequency should remain constant over a significant amount of time. Any deviations that could effect the supply sensitivity measurement will be detected during the forward path leakage tests. In many cases deviations will indicate a faulty CP-PLL. Therefore, is intended that any supply immunity tests would be carried out after any open loop deviation tests.

3.1. Frequency measurement details.

The basic methodology behind the test approach is to add a frequency counter to the output of the VCO and take two sets of successive frequency count measurements over a certain time period. The two sets of successive frequency counts are constantly offset in time by τ. Post processing of the frequency samples is carried out as follows:

1. Normalisation of the frequency count values to 1LSB (see (1) below).
2. Multiplication and averaging of sample set 1 and sample set 2 over the full record length.
3. Expansion of the record length by sequence repetition.
4. Taking the FFT of the results of step 2 to produce a power spectrum plot.

If the noise is stationary, the procedure in step 2 will effectively produce the auto correlation of the frequency count values. True monitoring of periodic noise components using this technique would require that τ could be varied across the full record length. However, for this paper and to keep the possible circuitry simple it was initially decided to investigate if any degradation could be detected using a fixed value for τ. Experiments have been carried out using ideal behavioural models for the samplers and frequency counters. However, possible hardware consisting of a frequency counter and a single delay element could be

implemented on chip and this is currently under investigation. The count values could be ported off chip for post processing. In addition, further delay elements could be introduced if required.
A block diagram of the envisaged circuitry is shown in figure 5.

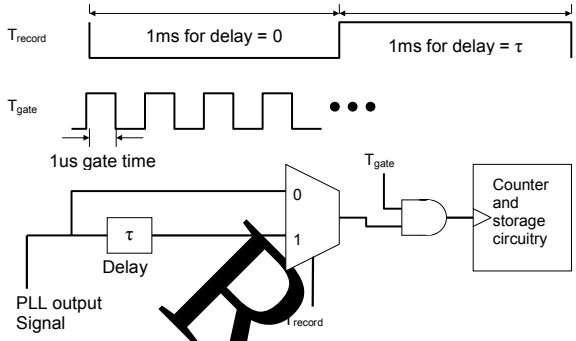

Figure 5 Test measurement procedure.

Values used for the initial investigations are provided in table 3.

Parameter	Value
T_{record}	1ms (2ms for successive records)
T_{gate}	1us
N (number of frequency counts)	1000
Expanded Sequence length	200000
τ	500ps
1 LSB	≈3.73mv

Table 3 Measurement parameters.

The gate time chosen was a trade off between simulation time, and the required LSB resolution. It was found from observation of the simulation results that frequency count deviations for the deterministic noise were periodic in nature. This fact was used to allow expansion of the recorded record length for post processing.

In [2], VCO circuits and sampling structures were proposed for the measurement of on-chip analogue or digital supply noise. In the approach, the VCO control input was connected to the relevant measurement point. Here the technique is being used to measure the immunity of the CP-PLLs VCO structure. In this situation, deviations in the output frequency could occur from control voltage, or substrate and supply deviations caused due to externally coupled noise. In an ideal situation, the VCO frequency will only be dependant on the control input. However, if the VCO frequency is dependant upon any of the other mentioned mechanisms, these can be viewed as additional control terminals. For a constant value applied to the control voltage terminal the LSB will be defined as the minimum voltage change that can cause a 1 digit change in a count value over the predefined gate time. This value is related to K_{vco} and the measurement interval as follows.

$$1LSB = \frac{1}{K_{vco} \cdot T_{gate}} \qquad (1)$$

If the technique is used directly for noise measurement (1) is directly applicable. If however, the technique is used for supply immunity (1) will provide an indication of how well the VCO structures are decoupled from externally generated noise.
For the CP-PLL in question over a frequency count interval of 1us the LSB is approximately 3.72mv (see table 1 values and equation 1). Deviation in this value will provide direct indication of the VCO supply immunity.

4. Initial experiments.

This section shows initial simulated measurement results produced from the procedure outlined in section 3. Injected noise values outlined in table 2 were used. Identical procedures were carried out for the closed loop CP-PLL and open loop VCO.
In addition, to the values stated previously, random supply noise with amplitude of 103mV was also injected into the closed loop CP-PLL. The results are shown in figure 6.

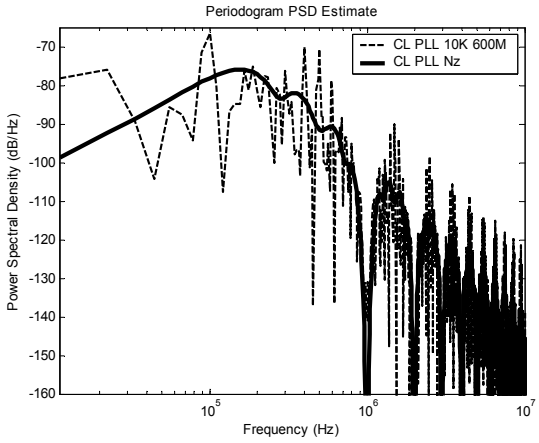

Figure 6 Closed loop CP-PLL with 103 mV random noise

From the solid plot of figure 6, the noise shaping properties of the closed loop PLL can be clearly seen. The peak in the response occurs at approximately 150 KHz, which corresponds with the initial estimations for ω_n that were provided in table 1. Figure 6 also shows a dashed plot for deterministic noise components over a range of 10 KHz to 600 MHz (see table 2). The deterministic components in the output spectrum can be seen at 10 KHz and 100 KHz.
Figure 7 shows measurements taken for the closed loop CP-PLL and open loop VCO. Figure 7 illustrates the

effect of noise components within the loop bandwidth. To show the effect of the closed loop PLL tracking the 10 KHz component, the plots are taken over a range of 40 KHz to 1 MHz.

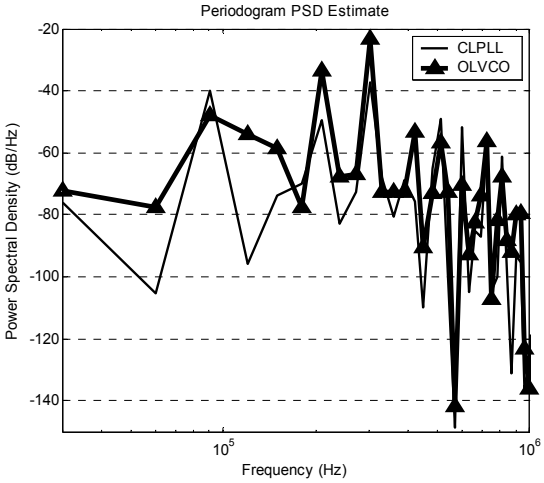

Figure 7 PSD plot for noise components from 10 KHz to 600 MHz (see table 2 also)

From the plots of figure 7 it can be seen that the open loop VCO is generally more sensitive to the injected noise than the Closed loop PLL. However it can also be seen that the closed loop CP-PLL attempts to track the noise component at 100 KHz within the loop bandwidth. This is shown by the amplification of the peak at 100 KHz. Further statistical measurements taken upon the data show that average of the closed loop CP-PLL data is approximately 9dB below that of the open loop VCO. This provides some indication of the expected sensitization of the open loop VCO. However, with reference to figures 6 and 7, it is evident that the technique may be useful for identifying deterministic characteristics in the closed loop CP-PLLs output signal directly. For example, Figure 6 clearly identifies the difference in output spectrums for random noise and deterministic noise. In consequence, the sensitization process required to enable measurements on the open loop VCO may not be required.

The plots indicate that even a relatively small number of frequency count samples may be useful in revealing the effects of noise injection. However, it must be noted that the sensitivity of the procedure will be related primarily to the VCO gain and sensitivity. For these initial experiments, relatively high gain VCO structures were used (see table 1 and equation 1). In other applications lower gain VCO structures may be present. Therefore, to provide suitable measurement sensitivity, the measurement procedure will have to be carried out over a longer interval. At present, it is felt that the measurement techniques may be useful in a production test environment for direct comparison against measurement masks taken from correctly operating CP-PLL systems. The initial experiments show that the techniques may be useful in assessing a PLL system performance in the presence of externally coupled noise. Obviously, to fully analyse the effects of sampling, counting, and test access structures on the measurements, the techniques will require implementation and evaluation in physical hardware.

5. Conclusions and further work.

This paper has briefly discussed possible sensitivity issues relating to fully-embedded CP-PLLs. A description of CP-PLL simulation models used for experiments was also provided. In particular, focus was directed towards noise coupling into the voltage controlled oscillator structures. A frequency counting method was presented that appears to be applicable to detection of the CP-PLLs VCO operation in the presence of coupled noise. The results of initial analysis with this technique show that it may be useful for characterisation of the VCO and CP-PLL operation in the presence of noise. Further work will concentrate on refinement of the methods and analysis of possible methods for suitable test limit generation. In addition, following the initial simulation based analysis, it is intended that the methods will be evaluated on physical hardware.

Acknowledgements

Thanks to ISLI Livingston, Scotland for providing resources and support. Thanks also Agilent for a trial version of the ADVANCED DESIGN SYSTEM 2003A simulation and design package and to Dolphin Integration, Grenoble, Fr, for access to the SMASH™ simulation software.

References

[1] P Larson, "Measurements and Analysis of PLL Jitter Caused by Digital Switching Noise", IEEE Journal of Solid-State Circuits, July 2001, pp1113-1122

[2] A. Alon, V. Stojanovic, M. Horowitz, "Circuits and Techniques for High-Resolution Measurement of On-Chip Power Supply Noise", IEEE VLSI Test Symposium, 200

[3] B. Razavii .Ed, "Monolithic Phase-locked loops and clock recovery circuits" , IEEE press, ISBN 0-780 1149-3

[4] M.J. Burbidge, J. Tijou, F. Poullet, "Investigations For Minimum Invasion Digital Only Built In "Ramp" Based Test Techniques For Charge Pump PLL's", Journal of Electronic Testing Theory and Applications. (JETTA) Volume19, Issue 4, Kluwer Academic Publishers.

[5] M. J Burbidge, A. Richardson, A. Lechner. "Evaluation and Detection of Deterministic Jitter Causes in CP-PLL's due to macro level faults and Pre-Detection Using Simple Methods", 9th IEEE International Mixed Signal Test Workshop, June 25th 27th 2003

[6] R. E. Best, "Phase-Locked Loops; Design, Simulation and Applications", pub McGraw-Hill, Fourth Edition, 1999, ISBN 0-07-134903-0.

[7] F. M. Gardner, "Charge-Pump Phase-Locked Loops", IEEE Communications Transactions, vol. COM-28, pp. 1849-1858, Nov 1980.

[8] G A S Machado (Editor), "Low Power HF Microelectronics a Unified Approach", IEE Circuits and Systems Press, 1996, ISBN 0852968744