Development of a Remote Access Facility for a PLL Test Course

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***Abstract*— The aim of this paper is to discuss the rationale for, development, and use of a remote access experiment facility for use in the teaching and learning of microelectronic circuit design and test principles. In particular, the operation and test of a phase-locked loop (PLL) circuit is the primary focus. In this arrangement, a set of existing experiments for the learning of the principles of operation of the PLL have been updated for remote access capability via a standard internet link. This arrangement provides for a range of tests to be undertaken by a remote learner with access to the PLL test board arrangement. This arrangement has been achieved by the modification to an existing remote laboratory arrangement in order to facilitate access to the PLL test board.**

***Index Terms*—Remote laboratory, PLL, test**

I. INTRODUCTION

The role that distance learning [1, 2] now undertakes within the teaching and learning environments on a global scale has gained widespread acceptance over the last number of years. Today, both local (at presence) and distance learning provide a blended approach to support the learner in addressing their personal learning objectives and circumstances[1]. Textural based teaching material, enhanced with graphics and animation, is now supported through the use of remote experimentation [3, 4]. The development, use, and support of internet based remote engineering and scientific experimentation laboratories can significantly enhance the student's learning experience. However, building and running the infrastructure to support this, and allowing for useful experiments to be accessed by a remote learner, is a basic requirement. This paper will discuss the rationale for, development, and use a remote access experiment facility for use in the teaching and learning of microelectronic circuit design and test principles. In particular, the operation and test of a phase-locked loop (PLL) circuit [5-7] is the primary focus.

The PLL, see Fig. 1, is used in electronic and microelectronic circuits/systems for providing accurate timing/clock signal generation. The PLL is essentially a closed loop feedback control system and can, depending on the implementation, be compared and contrasted with classic feedback control systems, such as proportional plus integral (PI) feedback loops. Many key PLL references rely heavily on classic control system theory and they often provide mechanical analogies to help explain PLL operation. Many common control system design techniques, for instance, bode plots, step response plots, nyquist plots, and s-domain mapping, can be used to aid the engineer in realising a correct system PLL implementation. However, a PLL system differs in one significant aspect, which is that the inputs and outputs of the system are usually considered to be continuous periodic signals whose parameter changes are in terms of phase or frequency. This subtle difference can often lead to confusion in terms of teaching the subject. In consequence, it is beneficial to aid the students understanding with use of practical examples. The PLL architecture of Fig. 1 consists of an edge sensitive phase and frequency detector (PFD), a loop filter, and a voltage controlled oscillator (VCO). The PFD senses the relative timing differences between the edges of the reference-clock and feedback-clock and produces correction pulses that are proportional to the timing difference. The pulses are most commonly used to control current-sources, which charge or discharge a capacitor in the loop filter. The voltage at the output of the loop filter is applied to the input of the VCO, which then changes oscillation frequency as a function of its input voltage. Ideally when the feedback and reference signals are equivalent in terms of phase and frequency, the circuitry will operate in such a way as to maintain the loop filter voltage at a constant value. The total system therefore forms a feedback loop where the VCO is frequency and phase locked to the reference signal. Note that the divide-by-N counter allows the PLL system to produce an output signal whose frequency is a multiple of the reference signal frequency.

This circuit element can be sourced as either a discrete packaged integrated circuit (IC), or a macro cell within a larger system-on-a-chip (SoC) [8] design. However, the mixed-signal nature of the circuit operation can lead to difficulties for a learner to conceptualise circuit operation. It has a number of characteristics specific to this type of device that are only effectively introduced and understood through practical "*hands on*" experiments. An arrangement for the PLL has been realised [9] for use within an existing distance masters programme operated by the Institute for Systems Level Integration (ISLI) [10] based in Livingston, Scotland. The PLL experimentation was developed by Lancaster University [11], England, to provide a means in which to investigate the operation of the PLL as follows:

[1] This paper was originally presented at the Remote Experimentation and Virtual Instrumentation Symposium (REV 2005), Brasov, Romania, 28th-30th June 2005. This manuscript has been modified for presentation in this publication.

- Design architecture and principle of operation.
- Device test principles.
- Transient (time) related operation issues.

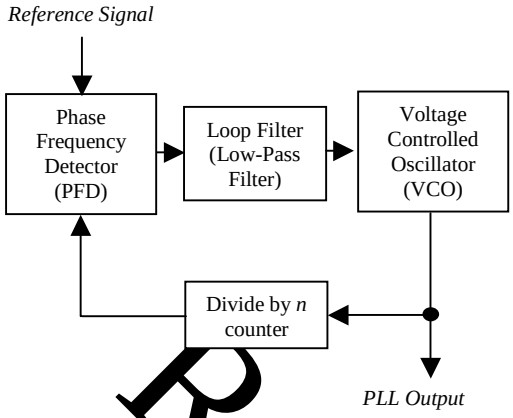

Figure 1. PLL structure

The original system was developed for at presence learning, where each student would be provided with the circuit board housing the PLL IC, along with a set of laboratory experimentation notes. The purpose of the work described in this paper was to consider the ability to provide a remote learning facility via an internet link as an alternative approach for the course delivery. In this case, a single PLL tester arrangement hardware was modified for connection to a remote laboratory developed and operated in the University of Limerick [12], Ireland.

As such, the project involved the following key points:

- Collaboration by three institutes on a cross-institute, cross-border arrangement.
- Development of a remote experiment facility based on an existing course structure and requirements.
- Re-design of the course structure and hardware in order to facilitate the remote learning scenario in addition to local (at presence) learning.
- Application of the remote experimentation facility on a trial basis.
- Collation of the results and experiences obtained.

The main part of this paper is structured to discuss the technological issues relating to the establishment of the remote facility. *Section II* will provide an overview of the PLL test board experimentation and local access mechanisms. This original arrangement was developed to provide a user with full control of the PLL features. *Section III* will highlight the modifications of the PLL tester hardware and interfacing to the PC based server arrangement. This was required to interface the hardware to the existing remote laboratory facility, using the standard interfacing approach adopted by the developers of the remote laboratory. The software system development is provided in *section IV*. *Section V* will present a case study access and the paper will be concluded in *section VI*.

II. Overview Of The PLL Board And Test Arrangement

The PLL synthesiser demonstration board arrangement is depicted in Fig. 2. The hardware was initially developed for use in a residential lab based course that utilised conventional bench top measurement equipment (power supply and oscilloscope). To facilitate measurement and injection of signals and modification of operational parameters, the hardware included various measurement points and preset switches. The PLL architecture chosen was a classic-digital integer-N architecture. The primary reason for choice of this architecture is that it is commonly used in a variety of applications and its basic operation is representative of a number of other architectures.

The block diagram of the original PLL board, shown in Fig. 2, highlights the measurement points and connection details that are also relevant for the remote adaptation. The PLL demonstrator board consists of the following elements:

- Main PLL circuit: This circuit is a Philips Semiconductors PLL [13] integrated circuit. Fig. 3 shows the pin-out for the 16-pin DIL package. The IC itself operates on a +5 V power supply and requires external resistors and capacitors in order to operate.
- A master oscillator provides the master timing (clock) signal for the system. The master oscillator frequency (*MREF*) was fixed at 1 MHz.
- The reference divider and feedback divider circuits consist of 8-bit terminal-counter circuits that can be manually controlled by an 8-way dip (dual in-line package) switch. These switches allow the input clock signal frequency to be divided by a maximum value of 255. In the remote access version of the hardware, the manual control switches are bypassed and controlled externally.
- The frequency-step control circuitry is used to toggle the least significant bit of the feedback divider counter. This can be used to enforce a frequency-step on the PLL output signal. The circuitry is bypassed in the modified circuit and the toggle signal is generated by external logic.
- The analogue VCO control voltage input is used to facilitate manual control of the VCO frequency (*Fout*). The change in output frequency with respect to change in input voltage can be used to determine the VCO gain characteristics.
- The analogue loop filter output voltage connection is used to monitor the transient characteristics of the PLL system as it is switched between two frequencies.

The switches and test points allow the student to carry out various experiments relating to steady state and transient operation of the PLL system. For the original (i.e. not remote) laboratory sessions, the test points allowed connection of an oscilloscope to various sections of the circuit. In addition, an external signal source could be connected the PLL reference input.

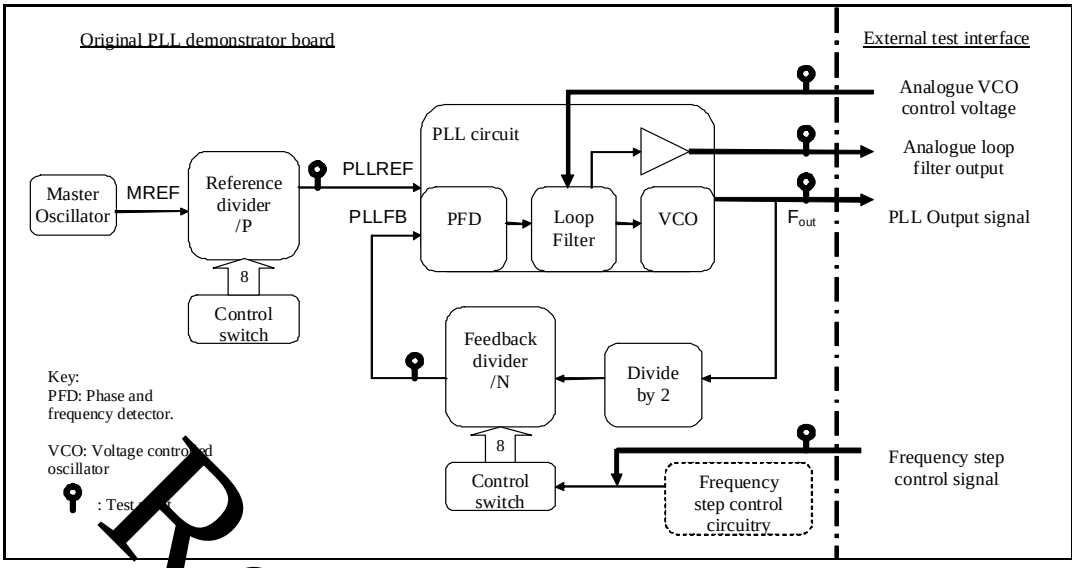

Figure 2. PLL board block diagram

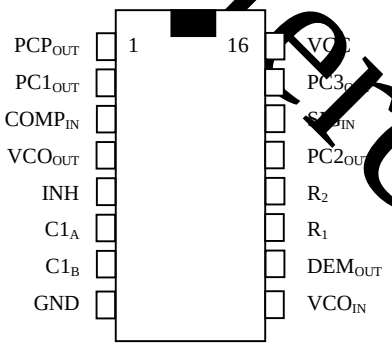

Figure 3. PLL pin-out

Although not shown in Fig. 2, switches were included to isolate the on-board reference oscillator from the external signal source. The control switches and test points included on the board can be used to carry out basic frequency divider setting tests, VCO gain measurement tests, transfer function monitoring tests and step response monitoring tests. A photograph of the board is shown in Fig. 4.

The 74HCT4046 PLL was chosen for various reasons, the principal ones being, architecture and features, availability, cost, and ease of integration onto the general purpose test board. The PLL IC is self-contained and includes three types of phase detectors (see Fig. 3), PC1 (an Exclusive-OR type), PC2 (PFD type), and PC3 (a JK-flip-flop type). PC2 (the PFD output) is used exclusively for the experiments explained in this paper. The main reason for this is that it is a representative example of a widely used circuit configuration. Additionally, the arrangement can still be used to generically explain useful system features such as step response and the system transfer function. Although only the PFD is used, the output can be disconnected and test points are included on the other phase detector output pins. This was done to allow use of alternative configurations at a later stage if desired. The PFD actually has two output pins available, PC2 is the proper or useful output and PCP is a derived output that can be used to provide a logical in-lock detection signal. The signal becomes 'high' when the PLL is in-lock and this signal is used to activate an LED (Light Emitting Diode) on the test board. In teaching situations, this function can be useful as an initial indicator of correct system operation. The PLL IC also includes a voltage controlled oscillator (VCO). The output frequency range versus input voltage of the VCO can be set using external components. The maximum frequency is approximately 17 MHz, but for the experimental board the maximum was set using external components to approximately 4 MHz. In the experiments and during normal operation, the PLL system parameters are changed to produce frequencies in the range of 2 MHz to 3 MHz. It must be mentioned that the use of relatively low frequencies eases the design and measurement process and allows standard digital components to be employed in the feedback path of the PLL circuit. Additionally, this low frequency configuration more than adequately emphasises many of the important characteristics that relate to very high performance PLL systems. Alteration of parameters is achieved by changing an 8-bit binary value of the manual control switches (see Fig. 3) connected to the control ports of the feedback and reference divider ICs. The divider ICs consist of 74HC4013 binary Up-Down counters connected in a frequency divider configuration. Initially, when the course was planned for at-presence learning, the use of programmable logic was considered for implementing the division circuitry. However, it was recognised that this approach may hide some of the circuit implementation detail from the student. In consequence, the decision was made to use small scale digital logic circuits (the counter IC's) for the circuit design so that the key building blocks of the PLL system would be clearly visible to the student. In the remote access implementation of the course material it may be valid and more convenient to use a programmable logic

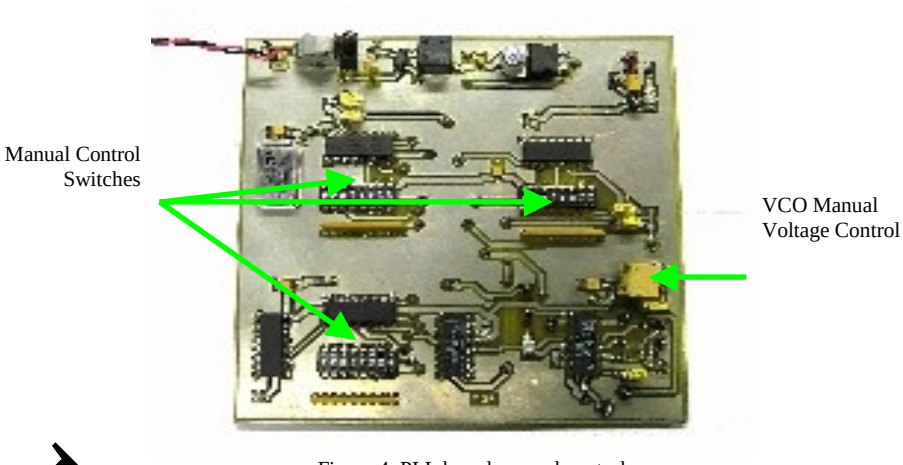

Figure 4. PLL board manual control

device (PLD) for the extra circuitry. In this case, graphical symbols representing the various system components could be implemented on the graphical user interface these could then be mapped to the internal logic blocks of the programmable logic device. One added advantage of using programmable logic is that the simple programmable logic techniques could be introduced into the tutorial material. Re-design of a version of the board using a programmable logic device is currently under consideration.

In addition to the physical hardware, a set of simulation models have been developed that mirror the operation of the PLL synthesizer system. The simulation models were originally developed to allow the students to become familiar with the measurement system prior to attending the laboratory sessions.

III. Modifying The Experiment For Remote Access

The web server arrangement [3] used for remote experimentation access is based on a standard desktop PC, see Fig. 5, the Apache Web Server [14], with PHP [15] scripting, a MySql [16] database and Visual Basic™ (VB) [17] application programs. This arrangement allows for Internet access (web page I/O for the user) and experimentation hardware access (for this arrangement, via the PC RS-232 serial port).

In order to connect the PLL board (Fig. 2) to the existing web server, it was necessary to provide an electrical connection to the PC via an additional interface circuit. This involved additional wire connections from the board to the interface circuitry effectively by-passing the local control circuitry. Whilst not an optimal approach, it was taken to minimise the required circuit modifications. Any further development would look to integrate all interface and PLL circuit functions onto a single board that is controllable directly at the board level or via a PC interface. The interface communicates with the PC via a standard PC interface (RS-232) serial port.

This arrangement facilitated the ability for ease of interfacing to the existing web server and also removed the need for custom internal interface hardware – so aiding the porting of the hardware to other PC systems and also allowing for:

- The original (at presence) operation of the board to be retained.
- Remote access via the internet (the purpose of this work).
- At presence operation via computer based learning (CBL) – either using a predefined software user interface or via an interface to be developed by the student.

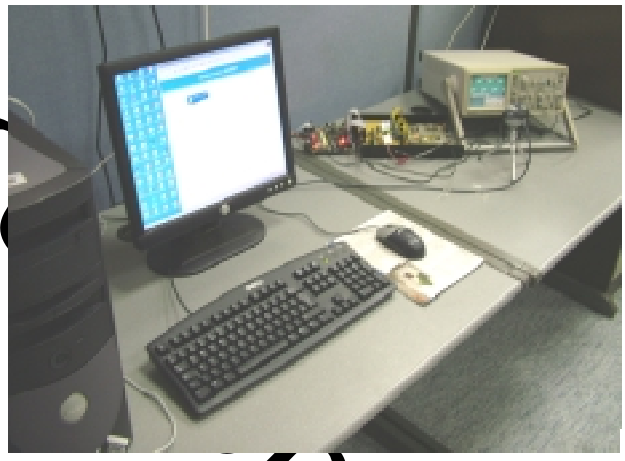

Figure 5. Web server arrangement

The above provides for flexibility in the end use of the hardware experimentation. Fig. 6 shows the basic arrangement adopted in this system. The digital electronic functions (UART, switch control, relay control, data capture control and data storage) are performed within a Spartan 3 (XC3S400) [18] device on an existing evaluation board [19]. This interfaces to the PLL board via a custom interface circuit that allows for digital to analogue (D/A) and analogue to digital (A/D) conversion as well as control of the PLL VCO (voltage controlled oscillator) voltage. Essentially, the web server interfaces to the same circuit control signals as would a local learner accessing the PLL board directly. This is also reflected in the design of the web server interface software.

The PLL output (oscillation frequency in the range 2 MHz to 3 MHz) is visually monitored using an oscilloscope and viewable by the remote user via the web

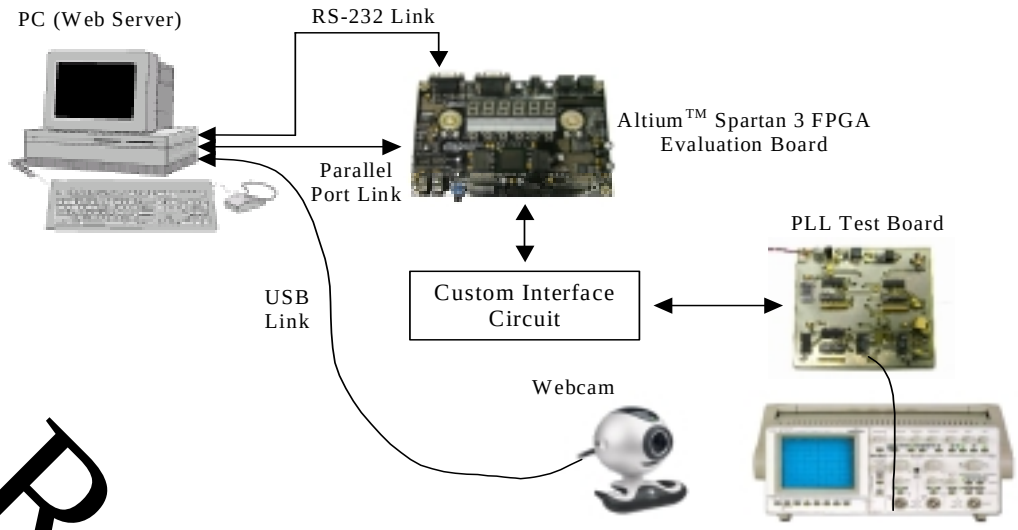

Figure 6. Experiment interface arrangement

cam [20], see Fig. 7. This was arranged to provide a "*hands-on feel*" of the experiment operation for the remote user. One limitation experienced is in the delay between submitting a change to the PLL and the monitoring of the web cam output. This is due to the arrangement where a queuing system has been established for experimentation access and jobs within the queue are operated on sequentially. It can be up to 1 minute (depending on the submission time and the number of users accessing the system) before the changes are acted on and noted on the web cam. Additionally, only one user can change the PLL settings in order for the oscilloscope output to be valid.

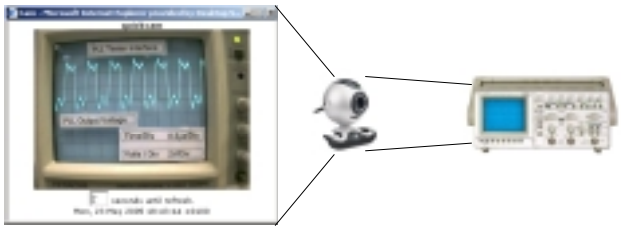

Figure 7. Webcam output

However, the web cam output provides count down clock which counts down to the window refresh time, along with information on the time the image was created. This feedback is used to identify any potential problems with the image update process within the web server software.

A second problem encountered related to the VCO output node and the monitoring the voltage appearing at the pin of the PLL IC. The addition of interconnect and an ADC sampling circuit produced an additional electrical load (mainly capacitive) which was noted during the testing phase. A potential problem due to the additional electrical load at this node was highlighted at the design stage and became apparent once the hardware had been designed and built. At this point, the effect noticed was that when changing between internal mode (the PLL is in closed-loop and the VCO voltage generated automatically) or external mode (the VCO voltage is generated through the use of a digital to analogue converter (DAC), see Fig. 8, an incorrect oscillation frequency occurred due to charge storage on capacitance in the circuit. This was resolved by effectively discharging the capacitance each time the PLL was accessed.

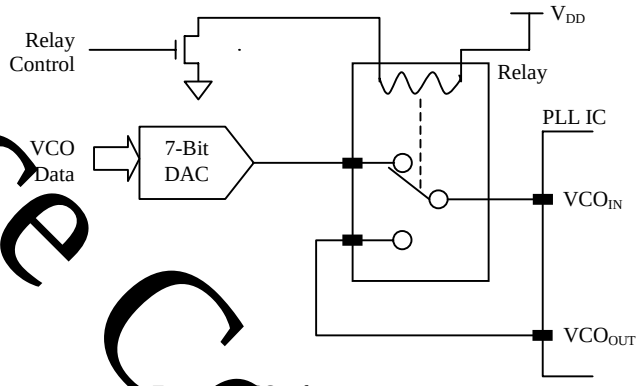

Figure 8. VCO voltage generation

A final part of the hardware set-up involves the programming of the FPGA. The web server administrator access has the capability to remotely reprogram the FPGA if so required. This is achieved either locally (at the web server PC) or remotely (via the administrator web access page). As such both the user and system administrator can be remotely located [3] from the web server and full access is available.

As with any experimentation arrangement, it is possible to provide the user with either simulation only results, actual hardware or a mixture of both, where:

- A simulation only system utilises a suitably defined model of the experiment and the user effectively controls the simulation operation by uploading simulation parameters from the user interface and monitors the simulation results.
- A hardware only system utilises the actual circuit under test and the user controls the operation of the hardware by uploading

control parameters from the user interface and monitors the results captured from the hardware.

- A mixture of the two above systems is possible where both actual hardware control and simulated results can be combined to produce an output for the user.

In the initial developed system, due to time constraints and unexpected problems encountered with the hardware development, it was chosen to utilise a mixture of actual hardware and simulation. In this, the user controlled the operation of the hardware by uploading control parameters from the user interface, was able to monitor the operation of the PLL via the web cam, but the returned results seen were simulated results based on previous experiments on the hardware connected to the web server. This provided a means in which the system could be developed in a modular manner and for it to be debugged and evaluated in a shorter time than if the full hardware was required to be fully operational. From a user perspective however, the results were no different as the results monitored were derived from the hardware at the time of the experimentation. However, for a fully operational system, the full hardware signal generation and results data capture was required.

IV. Design of the User Interface

The web interface to the experimentation is a link from an existing remote experimentation facility and is shown in Fig. 9. Here, the interface consists of 5 areas:

1. **Navigation Bar** – allows access to the experiment, results database and system login/logout.

2. **Image Panel** – graphical view of the hardware experimentation.

3. **Control Panel** – allows the user to control the settings of the reference divider, feedback divider and frequency step control switch, see Fig. 2.

4. **Information Panel** – access to the webcam, instructional videos, and PDF files for further information.

5. **Experiment Selection Panel** – select one of the 3 available experiments. The experiment notes are PDF files which are to be printed out and completed by the user.

The principle behind the user interface design was based on two key points:

1. To make the interface as straightforward and informative as possible.

2. To maintain the "*feel*" of the original PLL board. The interface provides the same user controls as the original board itself.

The user would follow the instructions provided in the laboratory notes and complete the control panel settings in order to set the required experimentation values. The results will be viewable by a change in the PLL frequency (web cam) and also in the results (ASCII text) files, seefFig. 10. The results are provided in basic text, *csv* (for importing into Microsoft® Excel), image plot and PDF output formats.

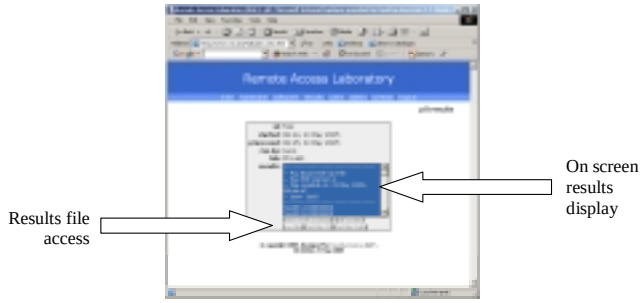

Figure 10. Results page

V. Example Use of the System

The user is capable of accessing 3 experiments, which each experiment aimed to provide an introduction to specific aspects of the PLL operation:

1. **Basic functional tests** - the user will set the reference and feedback divider ratios in order to set the PLL oscillation frequency.

2. **VCO gain measurement** - The user will control the (voltage controlled oscillator) frequency by setting the digital input word to a digital to analogue converter. The output of the DAC forms the VCO control voltage.

3. **Frequency step response** – this is used to measure the transient response of the PLL when a step change input occurs. The VCO voltage can be measured and the underdamped 2nd order response can be determined.

For example, consider the VCO voltage gain measurement. In this system, the voltage can be incremented in unit steps from 00_{10} to $+127_{10}$. This represents step changes in the VCO voltage of 39.06mV from 0V to 4.96V. It is then possible to create a plot of the VCO transfer curve (input voltage vs output frequency) and identify the limits of operation of the PLL. Fig. 11 identifies the key steps to be undertaken in this experiment. Fig. 12 shows the VCO transfer curve with the *x-axis* the DAC input code (00_{10} to $+127_{10}$) multiplied by 2, and the *y-axis* the PLL output frequency (in M Hz).

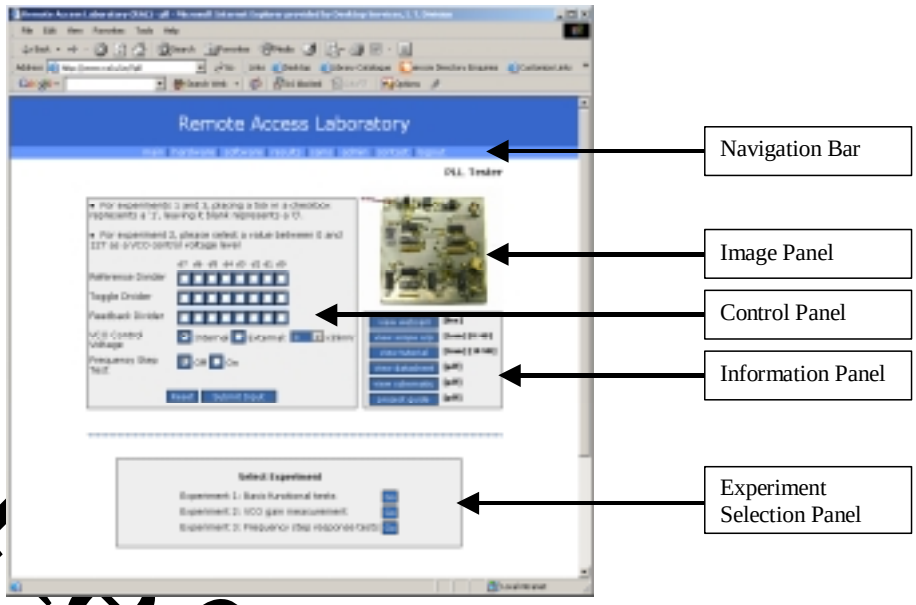

Figure 9. Web page user interface

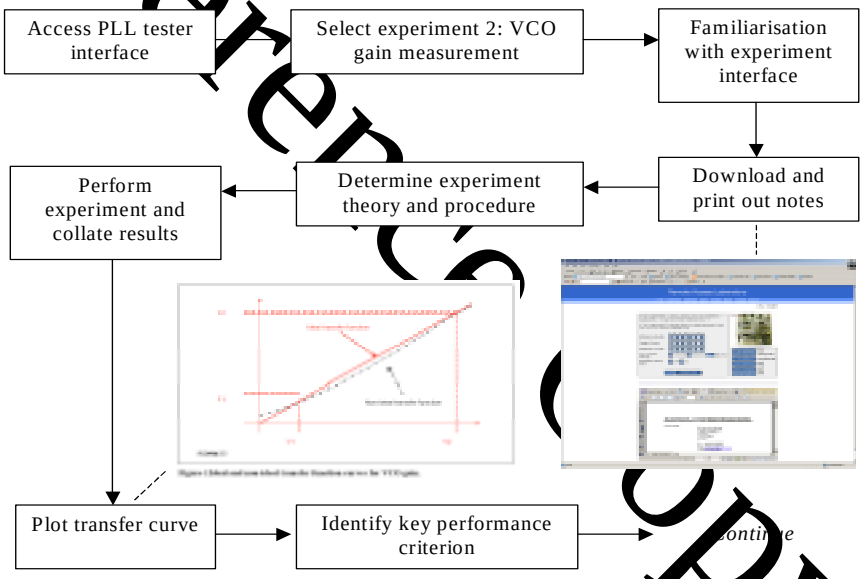

Figure 11. VCO step test procedure

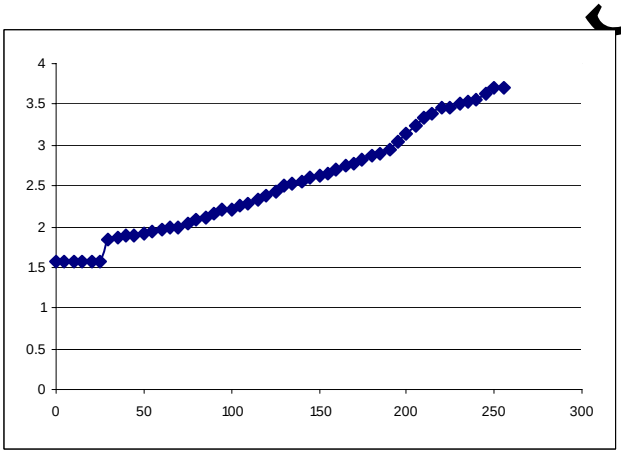

Figure 12. VCO transfer curve

VI. CONCLUSIONS AND FUTURE WORK

This paper had described the development and deployment of a remote experimentation facility for the learning of the operation of the phase locked loop (PLL). An existing experimentation arrangement was modified for connection to a web server arrangement and added to an existing remote experimentation facility. The original system was developed for at presence learning, where each student would be provided with the circuit board housing the PLL IC, along with a set of laboratory experimentation notes. The purpose of the work was to consider the ability to provide a remote learning facility via an internet link as an alternative approach for the course delivery.

The project required the collaboration of three institutes based in three different European countries. The technological issues to provide the facility were discussed and problems/solutions identified. Both hardware and software parts required modification/development in order to facilitate this work.

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